Vallen SysVeri

AMSY-5, AMSY-6 System Verification Software

User's Manual

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1 Purpose

Today's Acoustic Emission (AE) Systems are extremely flexible and multi-functional. A complete verification of all the functions and results in accordance with the manufacturer's specification overcharges the majority of system operators. The requirements of today's quality assurance systems to maintain documents of evidence for periodic verification and calibration of measurement equipment causes many operators to purchase expensive AE system verification services from the AE system manufacturer. Vallen SysVeri is an approach for a more efficient problem solution for users of AE systems model Vallen AMSY-5 or AMSY-6.
For using SysVeri with AMSY-6 please see chapter 14, "Appendix: Verification of AMSY-6".
Please contact sales@vallen.de if you need SysVeri documentation for AMSY4.

Vallen SysVeri is a software package containing two programs, VeriStimulator and VeriAnalyzer. The software and this documentation guide the operator through an automated verification process: A number of signal patterns are automatically created by a programmable signal generator, measured by the system under test, and verified by the VeriAnalyzer software. The VeriAnalyzer creates a verification report for the system and for each channel.
The main difference between "verification" and "calibration" is given by the request, that a "calibration" needs signal generators traceable to a standard, and the laboratory executing calibration services must be certified according to ISO 17025.

Vallen SysVeri, in combination with the required hardware accessories, makes system verification a fast and straight forward process that can be performed by most AE system operators even without the need of detailed system knowledge.

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2 Requirements

SysVeri requires a fully operational AE system model AMSY-5 or AMSY-6. The PC must have the following software installed:

- Microsoft Word version 2000 or later
- Vallen AE-Suite software release 2011.0303 or later, with software Key 'SysVeri' enabled.

For **system verification**, the following is also required:

- A programmable DC-calibrator with RS232 cable (CbD in Fig. 2), to stimulate the parametric inputs. SysVeri-software supports the control of model "M2000" over RS232. Software also supports the use of any manually controlled DC-Calibrator, e.g MIVC222-HPII. Required accuracy: 0,015% at 10V, output range: 0 to +10V.
- BNC cable, BNC-T-connectors and adapter for the calibrator output (usually 4mm banana sockets) to connect the DC-output voltage of the DC-calibrator to all parametric inputs in parallel.
- An already verified Reference Board to measure the calibration pulse:
  a) ASIP-2/A or ASIP-2/S board (with software releases higher than R2008.0101), or
  b) ASIPP board with dummy high-pass (HP4-dum) and dummy low-pass (TP4-dum) filter module.

For **AE-channel verification** the following is also required:

- A programmable Arbitrary Function Generator, to stimulate programmed waveforms of AE bursts. SysVeri-software supports control of model "Agilent 33220A" over Ethernet or USB, alternatively model "Agilent 33120A" over RS232 with appropriate cable to PC "CbF" in Fig. 2
- An appropriate cable to connect function generator with PC (RS232, USB, or Ethernet).
- With ASIP-2: DC-Bloc1: DC-Blocker for blocking the DC voltage supplied by the channel to protect the function generator
- A BNC cable to connect the function generator output (over a DC-Blocker for ASIP-2 verification) to the AC-input of one AE channel at a time.

The PC must offer a sufficient number of free LPTx / RS232 / USB / Ethernet ports to control the ET1 SysVeri-Adapter (LPT1), the Martel DC Calibrator (RS232) and the function generator (RS232 or USB or Ethernet). If two RS232 devices are to be used and there is only one free RS232 port, SysVeri can be used but with very few restrictions.

LPT1 is only used for control task (through ET1 adapter) during the acquisition of verification data and can be used afterwards to print the verification reports. If a printer is installed on this port, it must be disconnected, and the driver at least temporarily configured to use another port (e.g. LPT2) before VeriStimulator is started. If there are still problems, uninstall the printer driver. If there is only LPT1 and no LPT2 physically available and the printer shall be used again on LPT1, VeriStimulator must be closed, the cable to ET1 adapter be removed, the printer cable reinstalled and the printer re-configured to work on LPT1. If there is no LPT1 on your PC you might use a USB-to-Parallel-Port adapter.

The interconnection of the following parts can be seen in Fig. 2

Abbr: Description:
ET1: SysVeri-Adapter "ET1";
CbP: Printer cable (Sub-D-25-male to Sub-D-25-male)
CbE: Externals cable (16-pole flat female to SUB-D-15-female).
CbA: Alarm cable (10-pole flat-female to SUB-D-9-male)
CbD: cable to connect the DC calibrator Martel M200x with the RS232 of the control PC
CbF: cable to connect the function generator with the control PC, either RS232 or USB or Ethernet

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3 Overview

System Verification by using ***Vallen SysVeri*** is grouped into the following steps:

- AE system verification, and
- AE-channel verification.

3.1 System Verification

This step comprises the following verifications:

- Front panel - LEDs, external in-/outputs and parametric flags for “Alarm“, “Warning“, “SP0“, and “SP1“.
- Front panel - LED, external input and parametric flag for “Record Disable“.
- Measurement accuracy of external parameter inputs PA0 to PAx, x depends on system configuration and will be in range 1 to 7.
- Amplitude of calibration pulser, under manual and software control.

3.2 Channel Verification (ASIPP or ASIP-2)

This step comprises the following verifications:

- Channel internal timing parameters “Duration Discrimination Time”, “Rearm Time”;
- The burst-parameters amplitude, rise-time, duration, counts, energy, cascaded hits, cascaded counts, cascaded energy;
- The time driven parameters RMS, floating threshold.

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4 Basic Procedure for an AE-Channel Verification

Fig. 1 illustrates the basic procedure for a manually performed AE channel verification:

There must be a predefined list of test patterns to be verified.

A stimulus, usually an AE calibrator, must be set to create the predefined test patterns, step by step. Each pattern is fed into the equipment under verification, which converts the test signal to results. The operator reads the results, records them in a report and checks whether or not they meet the acceptance criteria.

Then the next test pattern will be processed until the list is completed.

Finally, the channel will be accepted, if all results meet the acceptance criteria, otherwise it will be rejected and needs repair or at least re-adjustment.

The automated AE-channel verification, as well as the verification of other parts of the system, will basically follow the same procedure.

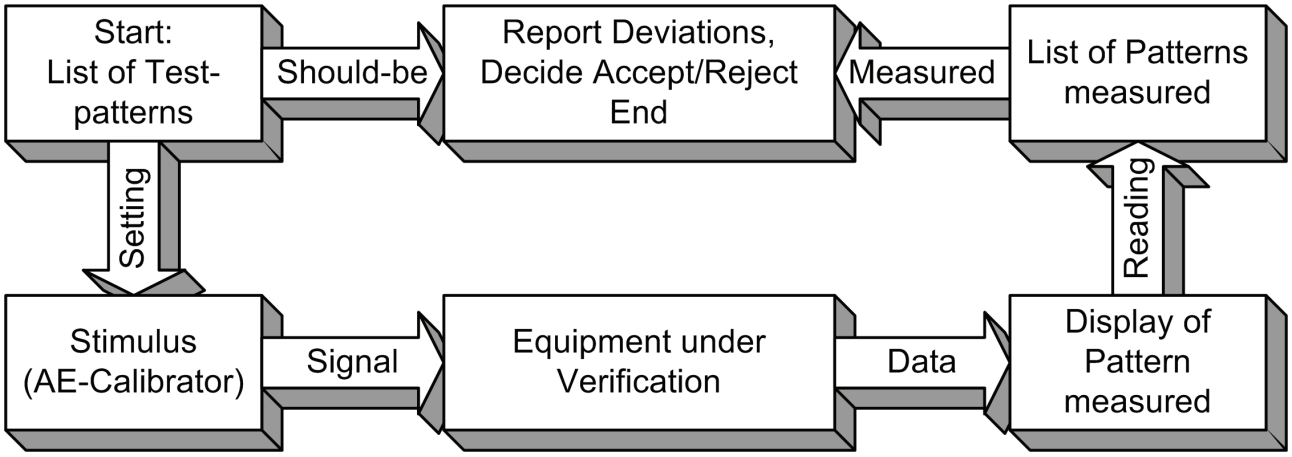

Fig 1: Basic Procedure for AE Channel Verification

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5 Hardware Set-up for the automated AE-System Verification

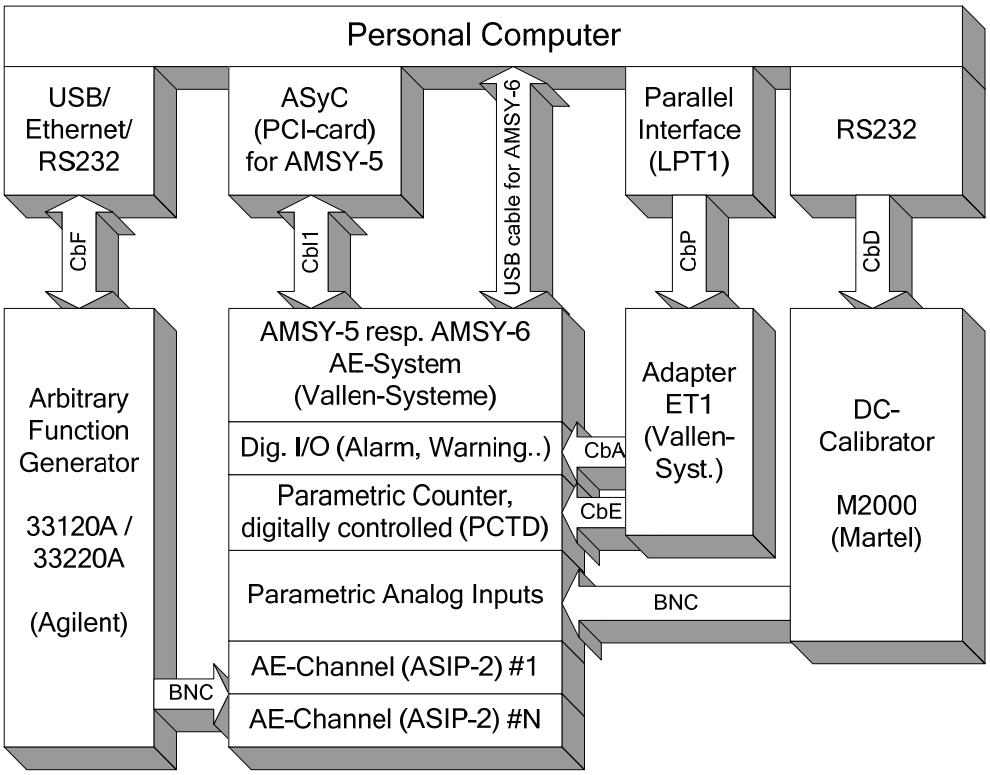

Fig. 2: SysVeri - Hardware Setup for an automated AE-System Verification

Fig. 2 shows the hardware setup for an automated AE-system verification. The PC controls the AE-system as usual. In case of AMSY-6 the connection to PC is done with an USB-cable, in case of AMSY-5 over a high-speed PCI-interface board (ASyC) For the channel verification, the PC also controls an arbitrary function generator (e.g. Agilent 33220A) to generate the pre-defined AE test patterns, and, over a parallel interface (LPT1), a parallel cable (CbP), and the ET1 Adapter, the AE-system inputs for data recording control, for a parametric counter and for additional I/O signals. For the verification of the parametric inputs, a DC-calibrator is controlled over a RS232 serial interface.
Attention: to protect the function generator against possible 28V DC output voltage of the AE-channel a DC-blocker should be used.

6 Software Component Interactions for the automated System and Channel Verification

The SysVeri software package consists of the programs VeriStimulator and VeriAnalyzer. VeriStimulator guides the operator through the data acquisition step where certain test signals are generated and recorded by the AMSY under test using the normal Vallen acquisition program. After the data acquisition step VeriAnalyzer compares the measured data with expected values and generates reports.

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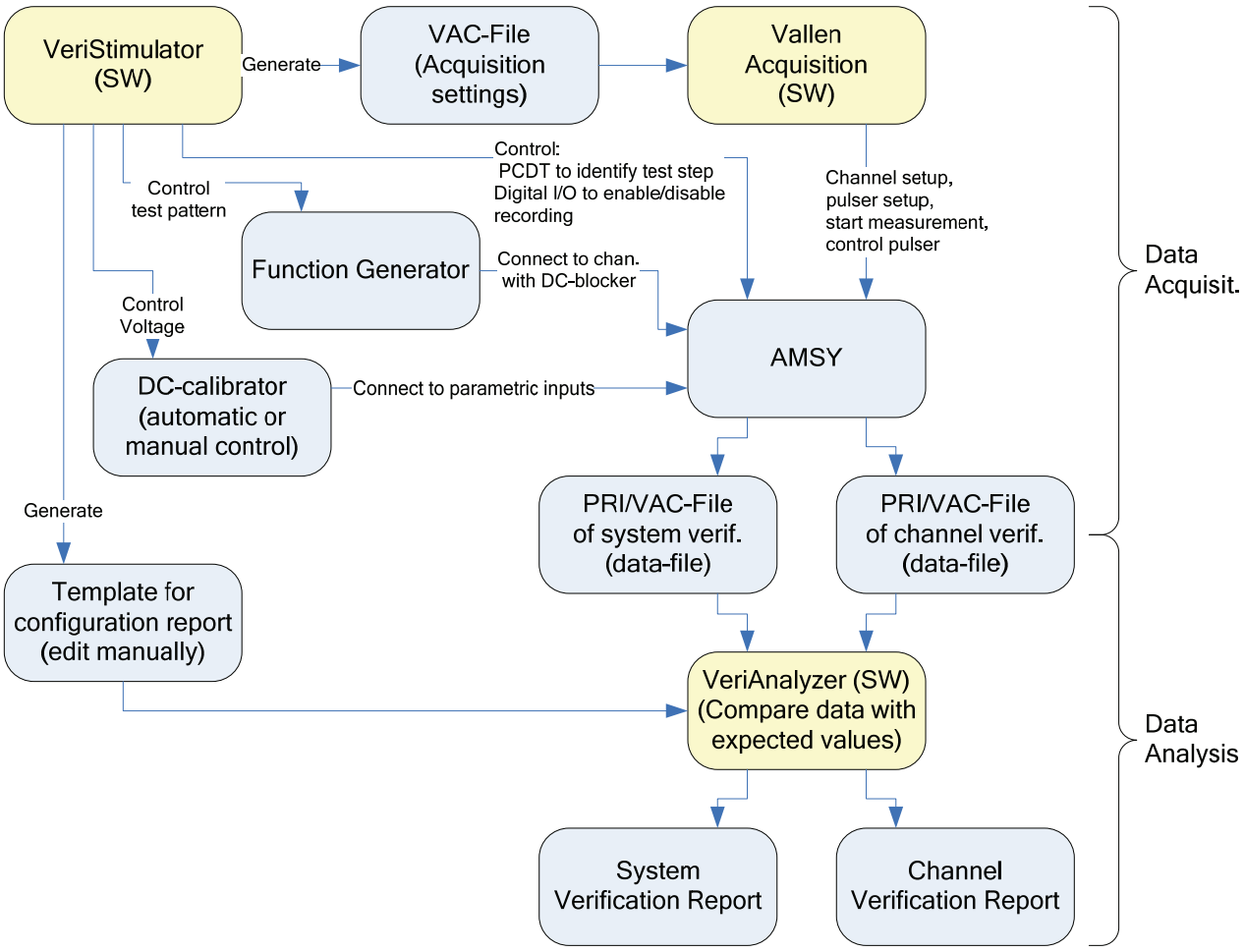

The figure above visualizes the software components (marked in yellow) used for system and channel verification together with their main interfaces. They are described in more detail in next sections.

6.1 VeriStimulator

This program controls the DC-calibrator, the arbitrary function generator and the parametric counter. The DC-Calibrator stimulates the analog inputs for external parameters, the function generator generates predefined test patterns, and the parametric counter identifies each test pattern on the data file for later analysis. The program guides the operator to make the needed connections.

6.2 Acquisition

This is the normal data acquisition program, which controls the AE system, receives the measured data and stores it on hard disk. It doesn't know that it is used in a verification mode. It performs as usual. This is possible due to the identification of each test pattern by a unique parametric counter value stimulated by VeriStimulator.

6.3 VeriAnalyzer

This program is called after all pattern stimulation for all parametric inputs and all AE channels have been completed. It reads the acquired data from hard disk, identifies each pattern by the parametric counter data and checks whether or not the measurements meet the acceptance criteria. It creates an easy readable system report and one report page per AE-channel.

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7 AE Test Signals and Result Examples

The automated verification process uses the following kinds of test signals which are stimulated by the arbitrary function generator under software control:

7.1 Single Dirac Pulse

This is a sharp pulse (Fig. 3), used to trigger a hit for passing administrative information (in the parametric counter PCTD) to the VeriAnalyzer software. Due to the wideband characteristics of a pulse, it will pass each frequency filter installed in the AE channel.

Such pulses are used

- To indicate the data format (version id) of VeriStimulator,
- To open or close a certain test series (e.g. the variation of a certain AE parameter).

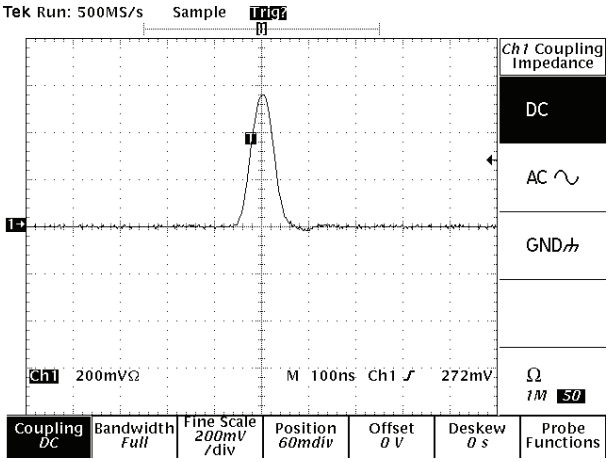

Fig. 3 Dirac Pulse, 50ns width (at 50% amp.)

See set 633 in Fig. 6. PCTD=18 initiates a series of duration varied hits. PCTD=2 closes the series, PCTD=70 to 86 point into a “should be” table of durations for this verification step.

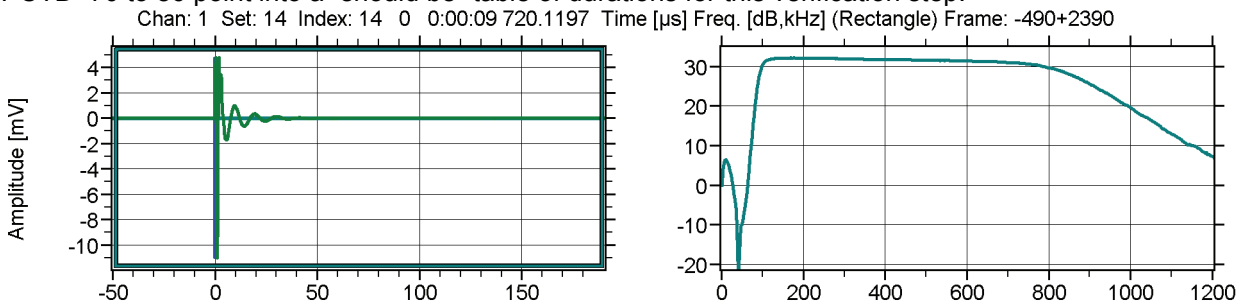

Fig. 4: ASIPP response (95-850kHz) to Dirac Pulse input. Left in time domain, right the FFT.

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7.2 Rectangular-shaped burst

Used to vary Duration and to check the parameters Duration, Energy, Counts. Problems: Settling behavior with overshoot at the beginning, and the ring-down behavior at the end (see Fig. 5) influence the AE parameters Peak Amplitude, Risetime, Duration, Energy, Counts. Needs some intelligent correction.

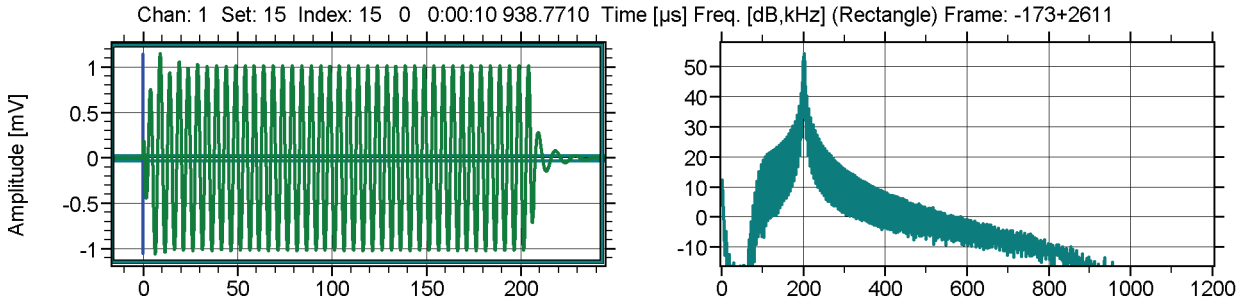

Fig. 5: ASIPP response (95-850kHz) to rectangular shaped sine wave burst.

7.3 Listing example for the duration variation test

Id	DSET	CHAN	PCTD	A [dB]	R [µs]	D [µs]	E [eu]	CNTS	Comment:
Ht	633	1	18	81,0	1,2	42,8	885E01	5	Dirac: Open
Ht	744	1	70	61,4	9,0	225,4	106E02	43	Testptrn #1
Ht	817	1	72	61,4	9,0	449,6	219E02	88	Testptrn #2
Ht	891	1	74	61,4	9,0	919,6	462E02	182	Testptrn #3
Ht	971	1	76	61,4	9,0	1919,2	979E02	382	Testptrn #4
Ht	1053	1	78	61,4	9,0	4024,0	207E03	802	Testptrn #5
Ht	1126	1	80	61,4	9,0	8483,2	437E03	1695	Testptrn #6
Ht	1199	1	82	61,4	9,0	17907,2	925E03	3580	Testptrn #7
Ht	1290	1	84	61,1	9,0	37836,8	195E04	7568	Testptrn #8
Ht	1362	1	86	61,4	9,0	80000,0	413E04	16000	Testptrn #9
Ht	1492	1	2	75,0	1,2	36,4	220E01	4	Dirac: Close

Fig. 6: Listing of a test with duration variations (initiated by PCTD=18 and closed by PCTD=2) see signal 3.1 above. PCTD = parametric counter digitally controlled. Each PCTD value identifies a test signal and the corresponding “should be” results

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7.4 Deviation diagram example for the duration variation test (Test #3)

The verification report shows a number of ”Deviation Diagrams”, which contain graphical and numerical results.

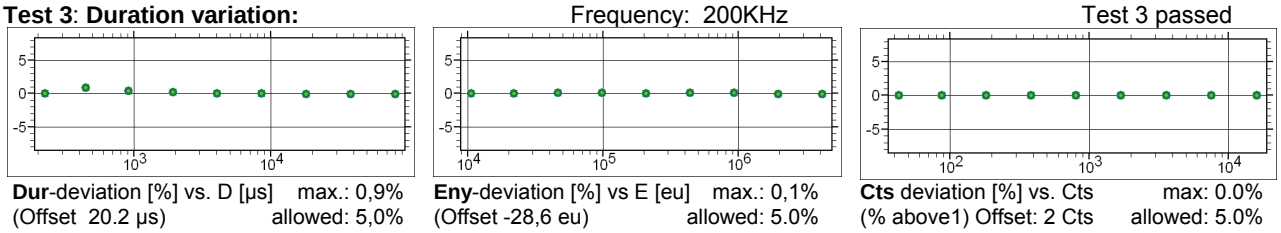
Test 3: Duration variation:
Frequency: 200KHz
Test 3 passed
Dur-deviation [%] vs. D [µs] max.: 0,9%
(Offset 20.2 µs) allowed: 5,0%
Eny-deviation [%] vs E [eu] max.: 0,1%
(Offset -28,6 eu) allowed: 5.0%
Cts deviation [%] vs. Cts max: 0.0%
(% above1) Offset: 2 Cts allowed: 5.0%

Fig. 7: Results in Fig. 6 shown in three ”deviation” diagrams.

The horizontal position of each dot in a diagram represents a ”should be” value, and the vertical position represents the deviation of the measured value from a ”should be” value, in percent or dB as given in the legend. The meaning of each diagram (axis results) and some additional numerical values are shown in different parts of the legend. The ”Offsets” indicated in the legends of Fig. 7 were determined by the deviation of the first (shortest) measured signal from the ”should be” values and applied to all 9 signals to correct the influence of the settling behavior and ring down effects.

7.5 Dirac Pulse Series

Series of short pulses are used to check duration discrimination and rearm timing (internal time parameters).

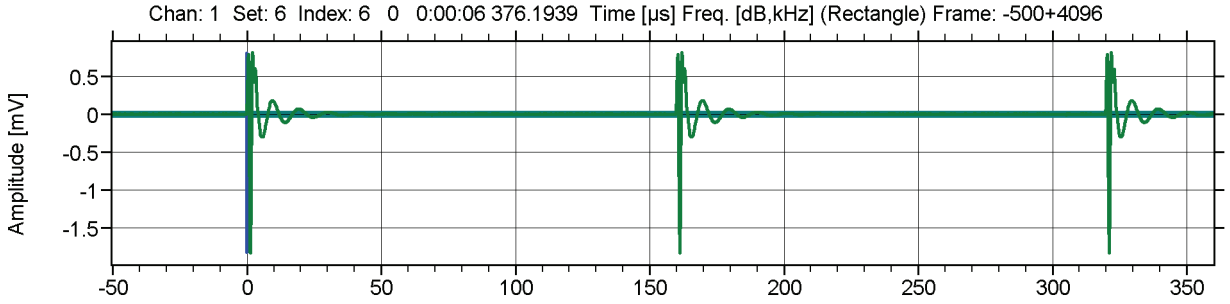

Fig. 8: Response to a series of Dirac Pulses

7.6 Sine-square-shaped burst

This is a sine wave burst in an envelope of a sine-square shape (Fig. 9).
This burst consist of 48 samples/sinewave and 41 sine waves for the burst, this gives a sequence of 1968 samples for the complete test signal. These sine-square-shaped test signals are used

- with frequency variation at a fixed amplitude to measure
- Frequency response (no need for transient recorder),
- Rise-time response;
- and with amplitude variation at fixed frequency to measure
- Peak amplitude response (linearity)
- Energy response (squared or non-squared).

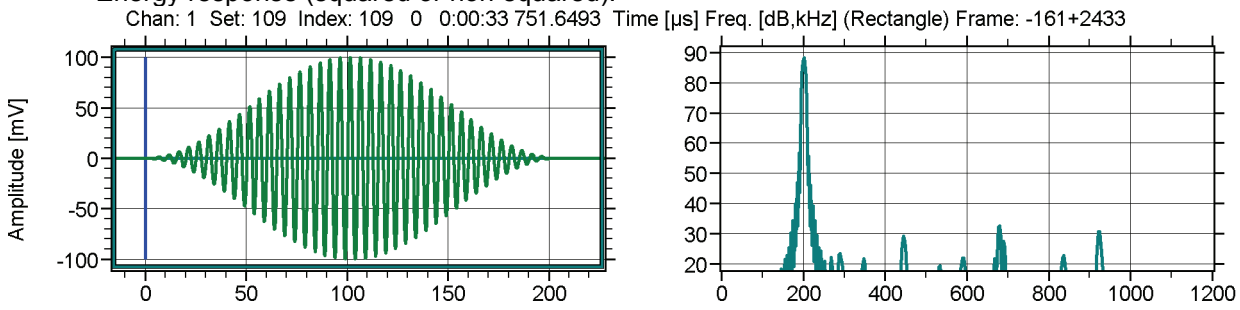

Fig. 9: Response to a sine-square-shaped burst.

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The impurities in the FFT (above 220kHz, right diagram) are produced by the function generator but do not disturb the results.

7.7 Data example: Frequency and rise time response

Fig. 10 shows results of test #4, where test signals of different frequencies (sine-square-shaped) were used. The upper diagram shows dB_{AE} values over the frequency. Above the diagram, the software reports the 3db bandwidth limits. The lower diagram shows the rise time-deviation vs. rise time (the measured vs. the should be values) of those signals that were measured with an amplitude above maximum – 1dB.

Since the rise time is defined as the time from first threshold crossing to peak amplitude detection, and the sine-square shaped test signal begins very smoothly, noise may contribute to some uncertainty of the exact time of the 1st threshold crossing. As can be seen in Fig. 9, the peak time is also difficult to determine. Due to these inherent uncertainties, a deviation of 10% for the rise time is shown as the allowed tolerance.

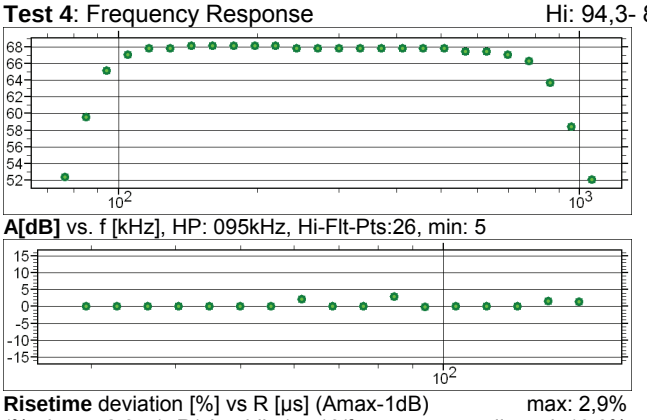
Test 4: Frequency Response
Hi: 94,3-
A[dB] vs. f [kHz], HP: 095kHz, Hi-Flt-Pts:26, min: 5
Risetime deviation [%] vs R [µs] (Amax-1dB)
max: 2,9%
(% above: 2,0µs) R(shouldbe) = 19/f
allowed: 10,0%

Fig. 10 Results of frequency variation:
Frequency response and rise time deviation

7.8 Data example: Amplitude variation, amplitude and energy response

Amplitude variations are obtained using sine-square-shaped signals, because these do not show the settling behavior as seen with rectangle shaped signals. Here, one difficulty was the limited dynamic range of the function generator, that is only programmable in a 46dB range, but we need to check a dynamic range of 70dB (30..100dB_{AE}). The increase of dynamic range for the function generator was solved by using a second sine-squared shape in a lower amplitude range.

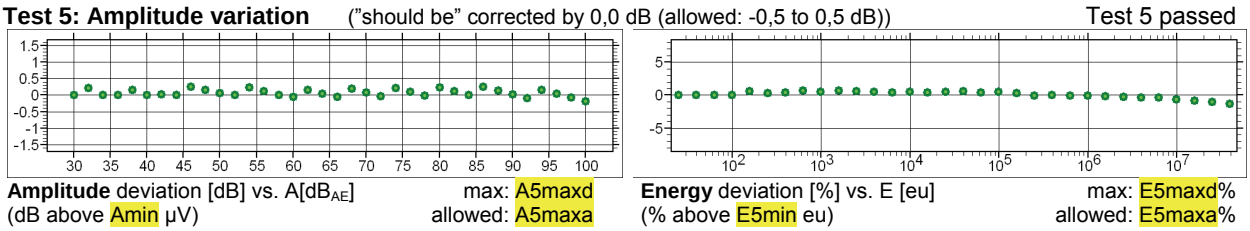
Test 5: Amplitude variation ("should be" corrected by 0,0 dB (allowed: -0,5 to 0,5 dB))
Test 5 passed
Amplitude deviation [dB] vs. A[dB_{AE}]
max: A5maxd
(dB above Amin µV)
allowed: A5maxa
Energy deviation [%] vs. E [eu]
max: E5maxd%
(% above E5min eu)
allowed: E5maxa%

Fig.11: Example for amplitude and energy deviation diagrams (Test #5 of verification).
A correction of the "should be" values for balanced positive and negative deviations, here 0dB, is shown above the diagram.

No external attenuator is needed and the full dynamic range can be tested without a change of the threshold setting.

Another difficulty can be shown in the listing of the amplitude-varied signals below. Usually, PCTD is incremented by 2 between two test signals. Below there are two occurrences where PCTD stayed constant (140, 150). Two unexpected signals of low amplitude (about 30dB) were triggered by noise from the function generator. However, those noise signals can be identified by the verification analyzer software and do not disturb the verification result as long as the signal with expected amplitude for each PCTD value can be found in the data.

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Data Example:

Id	DSET	CHAN	PCTD	A [dB]	R [µs]	D [µs]	E [eu]	CNTS	
Ht	3912	1	138	78,0	97,6	196,2	248E03	39	
Ht	3931	1	140	30,6	0,2	15,0	882E-3	1	←A=30,6dB
Ht	3933	1	140	80,2	97,8	196,4	392E03	39	
Ht	3969	1	142	82,1	97,8	198,6	622E03	40	
Ht	3989	1	144	84,0	97,8	198,8	986E03	40	
Ht	4009	1	146	86,3	99,4	200,8	156E04	40	
Ht	4029	1	148	88,1	99,8	201,2	247E04	40	
Ht	4048	1	150	31,3	0,2	57,4	592E-3	1	←A=31,3dB
Ht	4067	1	150	90,0	99,8	201,4	391E04	40	
Ht	4087	1	152	91,9	100,0	201,8	620E04	40	
Ht	4108	1	154	94,2	100,0	202,2	980E04	40	
Ht	4146	1	156	96,0	101,4	205,4	155E05	41	
Ht	4165	1	158	97,9	101,6	210,8	245E05	42	
Ht	4202	1	160	99,8	104,2	212,8	387E05	42	

Fig. 12: Listing of Test #5:
Amplitude variation in 2dB steps (Extract).
Problem: False hits (A < 32dB) triggered by noise of function generator.
Such noise is eliminated by VeriAnalyzer, because only the last hit of PCTD-ID counts.

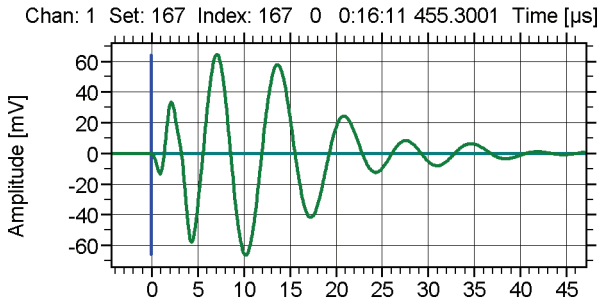

Fig. 13: Calibration Pulse Response

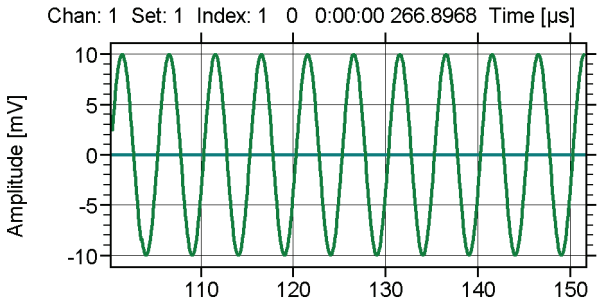

Fig. 14: Continuous sine wave

7.9 Calibration Pulse Response

This test signal (Fig. 13 shows the response) comes from the system internal calibration pulse generator and is only used to check whether the calibration pulse works as expected. There is no accuracy check required, because the pulse signal is checked by using a Reference Board (see section 3.1) during the system verification run. A Reference Board is needed because the filter configuration of the ASIP board can have a big influence on the measured calibration pulse amplitude.

7.10 Continuous sine wave

This test signal (Fig. 14) is used to verify the accuracy of background noise measurement and the floating threshold behavior. Due to the limited dynamic range of the function generator, 300µV_{RMS} is the lowest level that can be verified.

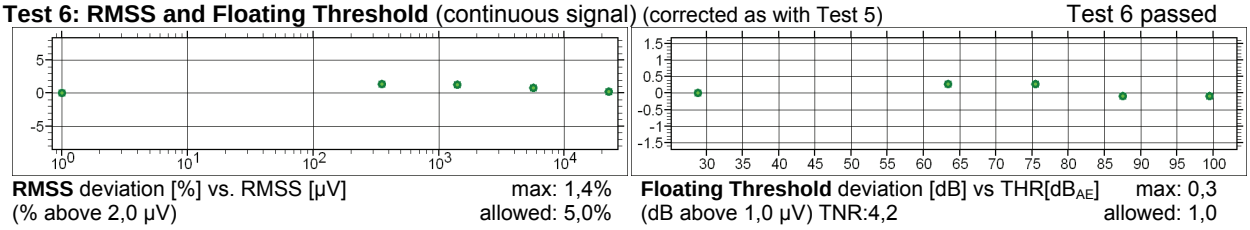
Test 6: RMSS and Floating Threshold (continuous signal) (corrected as with Test 5)
Test 6 passed
RMSS deviation [%] vs. RMSS [µV]
max: 1,4%
(% above 2,0 µV)
allowed: 5,0%
Floating Threshold deviation [dB] vs THR[dB$_{AE}$]
max: 0,3
(dB above 1,0 µV) TNR:4,2
allowed: 1,0

Fig. 15: Result of verification of background noise and floating threshold behavior (Test #6)

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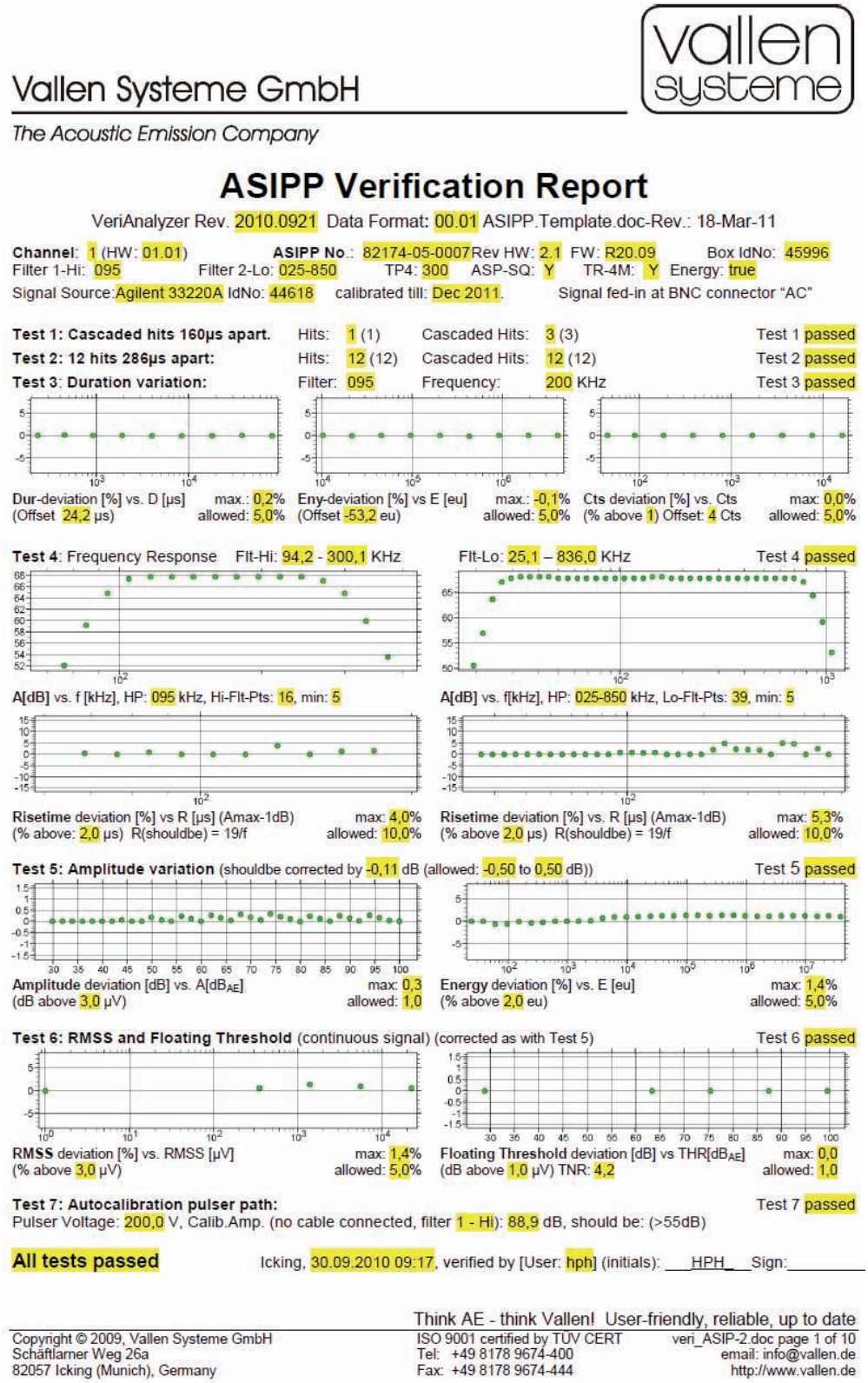
7.11 Example of an Channel Verification Report

Fig. 16 shows an example of an automatically generated AE channel verification report. It is derived from a word template. The yellow fields are place holders and the results were filled in by VeriAnalyzer.



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ASIPP Verification Report

VeriAnalyzer Rev. 2010.0921 Data Format: 00.01 ASIPP.Template.doc-Rev.: 18-Mar-11

Channel: 1 (HW: 01.01) **ASIPP No**.: 82174-05-0007 Rev HW: 2.1 FW: R20.09 Box IdNo: 45996
Filter 1-Hi: 095 Filter 2-Lo: 025-850 TP4: 300 ASP-SQ: Y TR-4M: Y Energy: true
Signal Source: Agilent 33220A IdNo: 44618 calibrated till: Dec 2011. Signal fed-in at BNC connector "AC"

Test 1: Cascaded hits 160µs apart. Hits: 1 (1) Cascaded Hits: 3 (3) Test 1 passed
Test 2: 12 hits 286µs apart: Hits: 12 (12) Cascaded Hits: 12 (12) Test 2 passed
Test 3: Duration variation: Filter: 095 Frequency: 200 KHz Test 3 passed

Dur-deviation [%] vs. D [µs] max.: 0,2% (Offset 24,2 µs) allowed: 5,0%
Eny-deviation [%] vs E [eu] max.: -0,1% (Offset -53,2 eu) allowed: 5,0%
Cts deviation [%] vs. Cts max: 0,0% (% above 1) Offset: 4 Cts allowed: 5,0%

Test 4: Frequency Response Flt-Hi: 94,2 - 300,1 KHz Flt-Lo: 25,1 – 836,0 KHz Test 4 passed

A[dB] vs. f [kHz], HP: 095 kHz, Hi-Flt-Pts: 16, min: 5
A[dB] vs. f[kHz], HP: 025-850 kHz, Lo-Flt-Pts: 39, min: 5

Risetime deviation [%] vs R [µs] (Amax-1dB) max: 4,0% (% above: 2,0 µs) R(shouldbe) = 19/f allowed: 10,0%
Risetime deviation [%] vs. R [µs] (Amax-1dB) max: 5,3% (% above 2,0 µs) R(shouldbe) = 19/f allowed: 10,0%

Test 5: Amplitude variation (shouldbe corrected by -0,11 dB (allowed: -0,50 to 0,50 dB)) Test 5 passed

Amplitude deviation [dB] vs. A[dB_{AE}] max: 0,3 (dB above 3,0 µV) allowed: 1,0
Energy deviation [%] vs. E [eu] max: 1,4% (% above 2,0 eu) allowed: 5,0%

Test 6: RMSS and Floating Threshold (continuous signal) (corrected as with Test 5) Test 6 passed

RMSS deviation [%] vs. RMSS [µV] max: 1,4% (% above 3,0 µV) allowed: 5,0%
Floating Threshold deviation [dB] vs THR[dB_{AE}] max: 0,0 (dB above 1,0 µV) TNR: 4,2 allowed: 1,0

Test 7: Autocalibration pulser path: Test 7 passed
Pulser Voltage: 200,0 V, Calib.Amp. (no cable connected, filter 1 - Hi): 88,9 dB, should be: (>55dB)

All tests passed Icking, 30.09.2010 09:17, verified by [User: hph] (initials): ___HPH___ Sign:_____

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Fig. 16 Example of a Channel Verification Report

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7.12 Example of a System Verification Report

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The Acoustic Emission Company

AMSY-5 System Verification Report

VeriAnalyzer Revision 2010.0921 ; Data Format: 00.01; Sys.Template.Doc: 18-Mar-11

System Id No.	Model	PAX Count	Mapped to
45996	AMSY-5 M6-2	4	PA0-3

Reference ASIPP used for Pulsertest: Id No: 71798-02-0077

Pulser Verification:

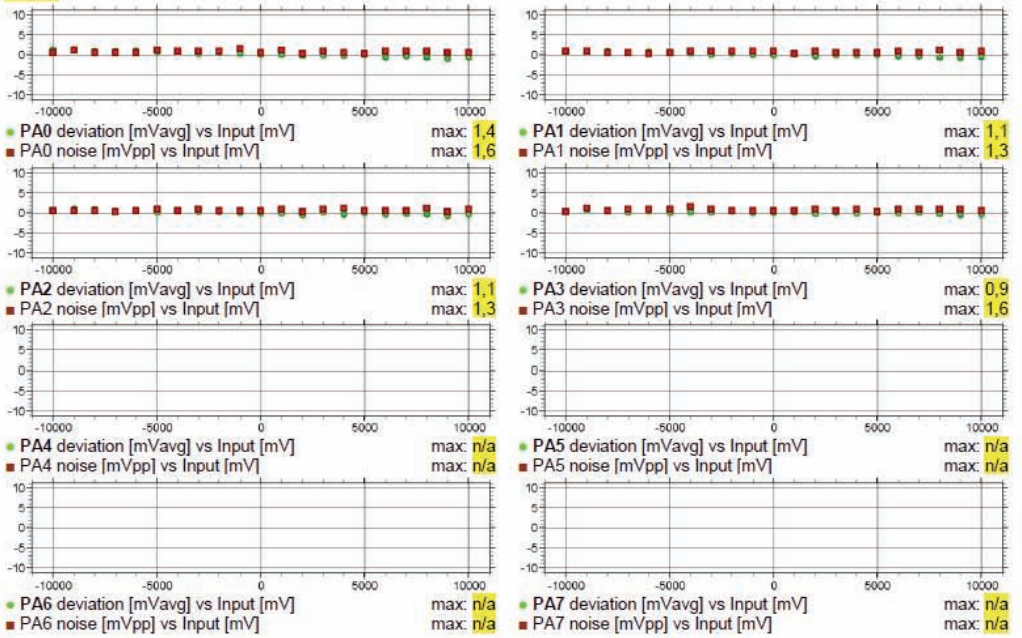
Pulser Amp.	Amp@ RefASIPP	Min Allowed	Max allowed	passed/failed:
Max (400V)	97,6 dB	96,0 dB	99,9 dB	passed
Min (4V)	45,2 dB	41,0 dB	50,0 dB	passed
Remote (200V)	90,8 dB	90,0 dB	94,0 dB	passed

Verification of I/O-Flag Function:

Stimulating Bits SP0, SP1, Warning, Alarm over alarm connector and verifying them in ParStatus — passed

Verifying Parametric Input Function:

Signal Source: Martel M2000, IdNo: 43071 calibrated till: Dec 2010. Signal fed-in to all PAx in parallel
Feeding 21 DC voltages from –10V to +10V in 1.0 V steps into all parametric inputs PA0 to PA3. — passed
Allowed Deviation: 25,0 [mVavg] (avg = Average); Allowed Noise: 5,0 [mVpp] (pp = Peak-Peak = Max-Min)


PA0 deviation [mVavg] vs Input [mV] max: 1,4
PA0 noise [mVpp] vs Input [mV] max: 1,6
PA1 deviation [mVavg] vs Input [mV] max: 1,1
PA1 noise [mVpp] vs Input [mV] max: 1,3
PA2 deviation [mVavg] vs Input [mV] max: 1,1
PA2 noise [mVpp] vs Input [mV] max: 1,3
PA3 deviation [mVavg] vs Input [mV] max: 0,9
PA3 noise [mVpp] vs Input [mV] max: 1,6
PA4 deviation [mVavg] vs Input [mV] max: n/a
PA4 noise [mVpp] vs Input [mV] max: n/a
PA5 deviation [mVavg] vs Input [mV] max: n/a
PA5 noise [mVpp] vs Input [mV] max: n/a
PA6 deviation [mVavg] vs Input [mV] max: n/a
PA6 noise [mVpp] vs Input [mV] max: n/a
PA7 deviation [mVavg] vs Input [mV] max: n/a
PA7 noise [mVpp] vs Input [mV] max: n/a

Date: 30.09.2010 08:55, verified by [User: hph] (initials): _HPH_ Sign:_____

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Fig. 17 Example of a System Verification Report

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After measuring the calibration pulse by using a Reference Board, the correct operation and routing of the 4 signals at the alarm connector (Alarm, Warning, SP0, SP1) are verified .
Then VeriStimulator controls a programmable DC-Calibrator (model Martel M2000) to generate accurate DC voltages that are fed into all parametric inputs in parallel. The green circles in the diagrams above indicate the deviation of the measured from the 'should be' values. The red squares indicate the peak-peak noise for each PA channel.

8 Templates

SysVeri interacts with a number of predefined templates that are described hereafter. These templates are installed in subdirectory c:\vallen\SysVeri by the installation program.

8.1 Configuration Report VeriCfg.doc

VeriCfg.doc resides on the application folder and is copied to a user defined folder and name by VeriStimulator. The operator shall fill-in the details of the configuration. VeriCfg.doc is used as a SOURCE for VeriStimulator. It contains all configuration information relevant for the verification process, such as:

- the type, ID number, and current address of the AE system boxes in which the AE channels are installed for verification ,
- The number of parametric inputs to be verified,
- The address of the Reference Board (see para 3.1) to be used for pulser verification
- the identification and recalibration dates of the used test signal generators,
  and for each AE channel:
- the ID number and current address of each AE channel plug-in,
- the channel's hardware and firmware revision,
- the installed options (squarer, transient recorder, and bandwidth limits of the frequency filters).

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AMSY-6/AMSY-5 Configuration Report

VeriCfg.doc 28 March 2011 Version 3.1

Signal Source used for PAx Input Stimulation: Martel M2000 IdNo: 43071 calibrated till: Dec 2011
Signal Source used for ASIPP-Verification: Agilent 33220A IdNo: 44618 calibrated till: Dec 2011

System Box Type	IdNo	RAD Adr (dec)	No of PA-Channels	Ref. ASIPP Id	Ref. ASIPP (Logical Adr)
AMSY-6 MBxx	xxxxx	01	x		
AMSY-6 EB21	xxxxx	02			
AMSY-5 Mxx-2	xxxxx	03	x		
AMSY-5 Testrack	42296	04		82174-05-001	123

ASIPP ASIP-2 Ch-No.	Test-No. / Vallen ID	Rev. HW	Rev. FW	ASP-SQ (Y/N)	OK	TR-4M TR-2 (Y/N)	OK	High-Pass 1 (Hi) HP4-	High-Pass 2 (Lo) HP4- / BP-	Low-Pass TP4-	Rem.	Verified
1	410	3.2	R0	Y		Y		095	n/a	850	⑤	
2	3500	4.3	R4	Y		Y		095	n/a	850	④	
3	708304003	1.1	R20.10	Y		Y		095	025-850	300	①②	
4	708304004	1.1	R20.10	Y		Y		095	025-850	300	①③	
5	82174-05-005	2.1	R20.10	Y		Y		095	025-850	300	①②	
6	82174-05-106	2.1	R20.10	Y		Y		095	025-850	300	①③	

Fig. 18: Extract of a Configuration Report (VeriCfg.doc) filled in by the operator with details about the devices used for test signal generation, the configuration of the system and the channels under verification.

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Details, such as HW (hardware revision) and FW (firmware revision) can be taken from the Vallen Systeme Configuration Sheet that comes with each system or from the software tool HW Reporter which you find on the Vallen Control Panel.

8.2 Sys.Template.doc and ASIPP.Template.doc

Sys.Template.doc is a Word file used by "VeriAnalyzer" for the generation of the System Verification Report. ASIPP.Template.doc is used for channel report generation (ASIPP as well as ASIP-2). The templates are installed in c:\vallen\SysVeri.

8.3 Customize Templates

Sys.Template.doc and ASIPP.Template.doc contain text marks and/or diagram place holders where VeriAnalyzer inserts results in numerical or graphical presentation. The Vallen header/footer and company logo can be replaced by that of the company performing the verification:

- make a backup of ASIPP.Template.doc from c:\vallen\SysVeri\
- open a new, empty WinWord document, insert the desired header/footer and make sure (page format) there is at least 17cm free width and 24,5cm free height for printouts.
- open C:\vallen\SysVeri\ASIPP.Template.doc and copy the body beginning with "Verification Report..." till "Sign___" into the new document.
- finally replace ASIPP.Template.doc in c:\vallen\SysVeri\ by the new document.

Then reports will be created with user-defined header/footer. None of the files should be write-protected.

9 Installation

IMPORTANT ! If you have modified templates (Sys.Template.doc, ASIPP.Template.doc, see 8.3): make a backup BEFORE starting a new installation because the existing templates are deleted during installation. After installing the software please

- make a backup of ASIPP.Template.doc from c:\vallen\SysVeri\
- open your modified template (from backup).
- open C:\vallen\SysVeri\ASIPP.Template.doc and copy the body beginning with "Verification Report..." till "Sign___" into your modified template.
- finally replace ASIPP.Template.doc in c:\vallen\SysVeri\ by the new document.

Vallen SysVeri is automatically installed with the AE Software Suite (Release 2005.04 on). The operation needs the SysVeri key enabled on the user's KeyFile. The software installation is described in the Info-Suite, chapter "Getting Started". VeriStimulator and VeriAnalyzer can be started from the Vallen Control Panel, Tab "Verification Tools".

If the function generator Agilent 33220A shall be controlled over an USB interface, the Agilent VISA drivers must be installed. See Info-Suite chapter AE Accessories, "Installing Agilent VISA drivers". Model 33220 can alternatively be controlled over Network, and Model 33120 can be controlled over RS232, both without a need to install the VISA drivers. The IP Address of the function generator can be obtained from its menu.

Fig. 19 – Reminder that waveforms must be loaded.

Each time VeriStimulator starts and finds a 33120A or 33220A function generator, you will see the window in Fig. 19. This is a reminder, that for the first time of using such a function generator, three waveforms must be loaded into the function generator's non-volatile memory.

Click on each of the three blue items "Upload…" on the left side of the VeriStimulator menu (see Fig. 20). This is only needed once per function generator, or, when one has overwritten one of the waveforms by another one.

The Martel DC Calibrator Model M2000 can only be controlled over RS232.

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VeriStimulator searches for both, the function generator and the DC Calibrator on all available interfaces. For offline use of SysVeri, no function generator and no DC Calibrator is needed.

10 SysVeri Step by Step

10.1 Reference Board

A reference board is needed for verification of the pulser (second step of the System Verification). The reference board has to be equipped with special filters.

ASIP-2 as reference board
In case of an ASIP-2 as reference board make sure that it is installed in the last system box as last board. Alternatively you can choose the last installed ASIP-2 in the last system box. Set one of its channels filters to 25-850kHz.

ASIPP as reference board
In case of an ASIPP, the HP – (high pass) and TP (low pass) filter have to be replaced by dummy filters. The reference board shall be installed in the last system box (last with respect to linking of the system boxes). If all slots are occupied by boards to be verified, remove the last board and replace it with the reference board. After the pulser step of the System Verification, before the operator starts the board verification, the reference board can be removed and the initial board reinstalled. (System must be powered down before a board is removed or installed).

As every board must be configured to a unique channel number, make sure the channel number of the reference board is unique in the AMSY-5 respectively AMSY-6 system box.
Channel number 60 is recommended for the Reference Board. Usually boards are configured in range 1 to 37 with AMSY-5, or 1 to 19 for AMSY-6 systems.

10.2 Connections

- Connect LPT1 of PC (printer port) to ET1-Adapter (using cable CbP)
- Connect ET1 external cable (CbE) to AMSY-5 master unit's external connector at the rear.
- Connect ET1 Alarm cable (CbA) to AMSY master unit's Alarm connector at the rear.
- Connect DC calibrator (serial interface) to PC.
- Connect Function generator (serial interface or USB or network) to PC.
  If the only free serial interface is occupied by the DC calibrator: System Verification can be done without function generator and Channel Verification can be done without DC-calibrator. Only one of them needs to be connected at a time.

Connecting several AMSY-chassis:

- AMSY-5: Connect all AMSY-5 boxes by using the foreseen cables CBL1-1.5 (PC to 1st AMSY5-box; length: 1.5m, CBL1-0.7 from box to box; length: 0.7m). The Pulse-BNC connectors of all boxes must be connected in parallel by using BNC cables and BNC-T-pieces. Make sure that the switch settings on rear panel of master/slave units are correct (master unit: switch 5 and 6 set to on; slave units: switch 5 and 6 set to off).
- AMSY-6: Please see AMSY-6 Operation Manual, chapter "Multi chassis setup" on how to connect several AMSY-6 chassis in case you want to test several chassis as one system.

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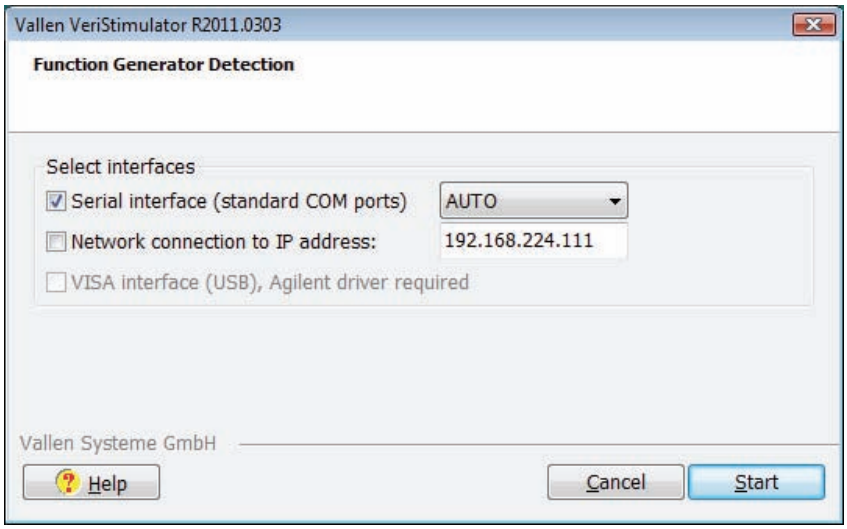
10.3 Starting VeriStimulator

In the VeriUtilities tab of the Vallen Control Panel start the VeriStimulator and follow the step-by-step instructions below.

After starting the VeriStimulartor it checks for the function generator which can be connected via serial interface, network or USB interface.

Choose your type of interface and continue with “Start”.

“Cancel” will skip the hardware detection.



10.3.1 Vallen VeriStimulator

The VeriStimulator main window is shown below. To the left hand side you find the group “Function Generator”. In the center of the window you find two tabs “Automatic Tests” and “Manual Control”. During the automated test routine you will only need the “Automatic Tests” tab.

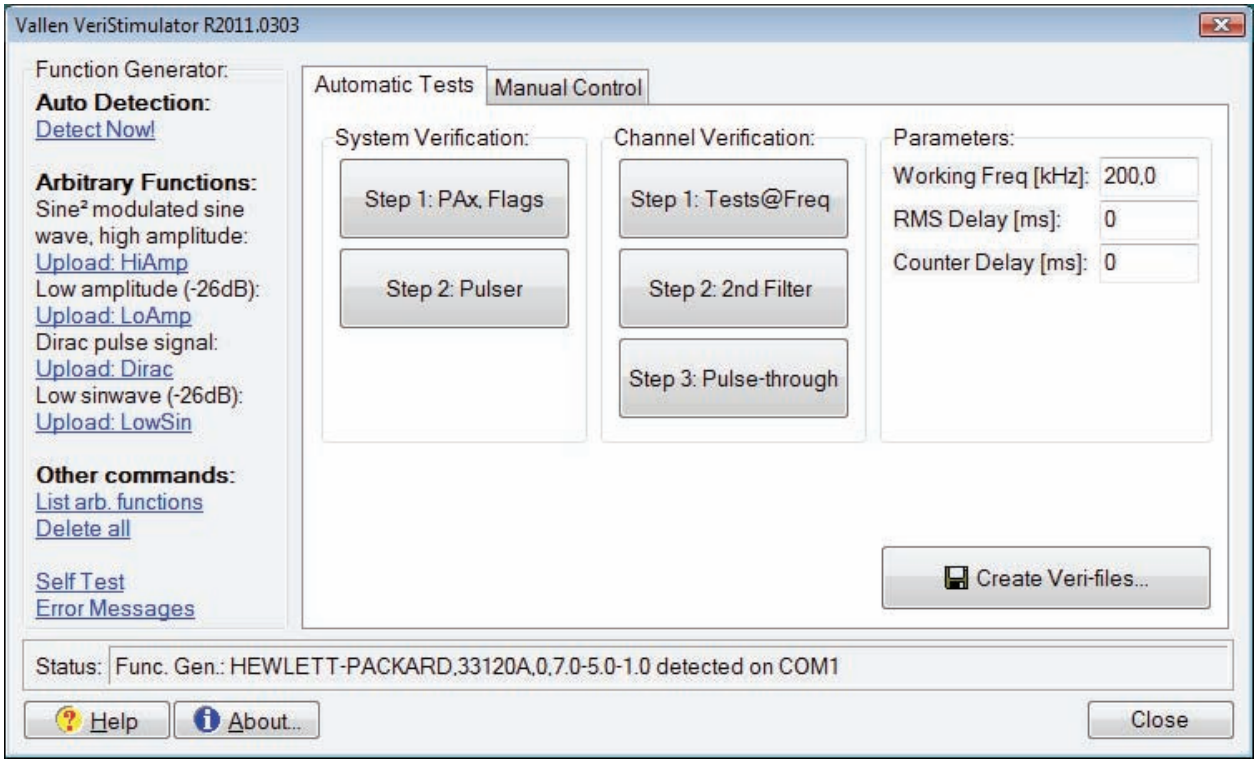


Fig. 20: Vallen VeriStimulator

Function Generator
The commands in the group “Function Generator” let you control the function generator.

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Command	Description
Detect Now!	Starts the hardware detection of the function generator. It is the same routine when you start the VeriStimulator
Upload: HiAmp Upload: LoAmp Upload: Dirac Upload: LowSin	These four commands let you upload the signals which are used during the verification steps. Please upload these signals when you are using the function generator for the very first time, or when the internal (non-volatile) memory of the function generator has been erased or used to store other signals.
List arb. functions	Lists the functions/signals that are in the function generator´s memory
Delete all	Deletes the memory of the function generator
Self Test	Performs a self test
Error Messages	Lists all the error messages of the function generator

Automatic Test
This tab is explained in great detail in the following sections. The buttons in “System Verification” and “Channel Verification” group guide you through a semi-automated process of verifying your AE-System. In the “Parameters” group you can specify the parameters for the SysVeri procedure.
Manual Control
In chapter 13 you can find out more about running the VeriStimulator in Manual Control mode.

10.3.2 Make Veri-Folder and create Veri-Files

To create the Veri-files click the button “Create Veri-files…”. First create the “Veri-Folder” in which all working files and results of the verification are stored; e.g. “D:\SysVeri\Identifier\” and specify a file name. This step creates a set of files, including

newname.VAC	acquisition settings
newname.VAE	VisualAE settings
newname.Cfg.doc	configuration file

10.4 Enter Configuration Report

Start Word and open “NewName.cfg.doc” (as created in VeriStimulator).

The file contains three groups of information to be entered (see also Fig. 18):

Group 1: Information about the used signal sources:

Signal Source used for PAx Input Stimulation:	Martel M2000	IdNo:	12345	calibrated till:	31.12.2012
Signal Source used for Channel-Verification:	Agilent 33220A	IdNo:	12345	calibrated till:	31.12.2012

The yellow fields indicate text to be transferred to the verification reports. To change such a text, double click on the yellow field. This opens a menu where you can change the text in item “Standard text”. Do not delete such a yellow field; this would cause improper function of the VeriAnalyzer software.

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Group 2: Information about the system box(es), parametric channels and the Reference Board.

System Box Type	IdNo	RAD Addr (dezimal)	No of PA-Channels	Ref. Board Id	Ref. Channel (Log. number)
*A1 (Master)	*B1	*C1	*D1	(*E1)	(*F1)
*A2	*B2	*C2	(*D2)	(*E2)	(*F2)
*A3	*B3	*C3	(*D3)	(*E3)	(*F3)
*A4	*B4	*C4	(*D4)	(*E4)	(*F4)

Up to four system boxes can be specified, one box per line. Field *A1 must indicate the master, which is the box with the lowest RAD address. Additional boxes shall be defined in the sequence of their RAD address.

Parametric inputs of the first box are mapped to PA0-PAx, where X is equal to "*D1-1". With AMSY-5, parametric inputs in the second box are mapped to PAy-PAz. Where y corresponds to *D1 and z to "*D1+*D2-1", etc., up to PA7.

If less than 4 boxes are used for verification, the corresponding lines must be empty.

The following information shall be entered into the fields:

*Ax Type of system box: e.g. AMSY-5 M6/M6-2, M16/M16-2, M37/M37-2 or AMSY-6 MB2, MB6, MB19. An extension unit, such as AMSY-5-E20/E20-2 or AMSY-6 EB21 can only be entered for *A2, *A3 or *A4.

*Bx the Id-number of the system box (see label on rear panel)

*Cx the rack driver address (RAD Addr) of the system box is configured on the rear panel. For AMSY-5 this is done by a slide switch: a value between 01 and 14. For AMSY-6 this is done by a rotating switch with value 1 to 9. Note: The box with lowest RAD address must be configured as Master box and all others as extension box. If switch setting is wrong, software will point that out to the operator. *Cx must be entered in increasing sequence. (*C4>*C3, *C3>*C2, *C2>*C1).

*Dx the number of parametric inputs in the box, usually 0, 2, 4 or 8. The fields D2 to D4 are considered up to a total number of 8.

Example: *D1 = 4, *D2 = *D3 = *D4 = 2 (4 par. inputs in box 1, 2 each in box 2-4).
This will cause the following mapping of parametric inputs:

Box	**PA channels built in**	**PA mapping in data file**
*A1 (Master)	PA0-3	PA0-3
*A2	PA0-1	PA4-5
*A3	PA0-1	PA6-7
*A4	PA0-1	Not available

*Ex a number or string that identifies the Reference Board. (see section 3.1) It is only used to verify the calibration pulse. If multiple boxes are used, it must be installed in the box that is farthest away from the master box. Three of the fields E1 to E4 and three of F1 to F4 must be empty, only the field belonging to the last box must contain this information. If all channel slots of the last box are occupied by normal boards, the board in the last slot must be exchanged against the Reference Board for the system verification part. The normal board can be reinstalled before the channel verification part.

*Fx the logical channel number assigned to the Reference Board: a value between 1 and 252. The user may remap any hardware address (consisting of the channel address and the RAD address) to any logical channel number between 1 and 252. (In Vallen Acquisition program, in step hardware detection select "Edit mode" to assign channel numbers.)

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Group 3: ASIP table: Information about the installed ASIPs (AE channel plug-in ASIPP or ASIP-2).

ASIPP **ASIP-2** Chan No.	Test-No. / Vallen ID	Rev. HW	Rev. FW	ASP-SQ (Y/N)	OK	TR-4M TR-2 (Y/N)	OK	High-Pass 1 (Hi1) HP4-	High-Pass 2 (Hi2) HP4- / BP-	Low-Pass (Lo) TP4-	Rem.	Verified
1	1234	4.3	R4	Y		Y		095	025-044	850	ASIPP4	
2	1234567890	1.1	R20.02	Y		Y		095	n/a	300	ASIP-2	
3	*B	*C	*D	*E		*F		*G	*H	*I		

For channel 1 the form above shows default values. They have to be replaced with the actual data for the installed ASIPP #1. (You can take these values from the configuration report that came with the system at time of delivery).

The meaning of fields *B to *I are described below:

*B ASIP-2: this is a number on a white label on the board. It can be obtained with the tool Hardware Reporter (Vallen Control Panel, tab 'Utilities') without removing the board,
ASIPP (single channel board, only supported in AMSY-5, not in AMSY-6): a hand written number on the board itself, remove the board to read that number (for safety cautions see your AMSY-5 Manual, section 'AMSY-5 Service Manual')

*C Hardware Revision (of ASIPP or digital board of ASIP2) is given on the Configuration Sheet that was shipped with the system (within the System User's Manual) or can be obtained with the tool Hardware Reporter (Vallen Control Panel, tab 'Utilities')

*D Firmware Revision can be obtained with the tool Hardware Reporter (Vallen Control Panel, tab 'Utilities')

*E N if no squarer installed, Y if squarer is installed. This information is shown during the hardware detection phase of Acquisition.

*F N if no TR-(transient recorder) module is installed, Y if TR-module is installed. To be seen in the Hardware Detection of Acquisition.

*G The cut-off frequency (-3dB) of the high pass 1 in kHz. See Configuration Sheet.

*H The cut-off frequency (-3dB) of the high-pass 2 in kHz. See Configuration Sheet.

*I The cut-off frequency (-3dB) of the low-pass module in kHz. See Configuration Sheet.
Note: The cut-off frequency in the configuration report is that of the filter module. Since the ASIPP frequency response slightly decreases towards higher frequencies, it is normal that the cutoff frequency reported in the Verification Report is lower than that reported for the filter module.

The empty fields have no influence on the verification.

The configuration report is read by the VeriAnalyzer program when all verification data have been acquired. It might be useful to make a hardcopy; you will need to know some contents later.

10.4.1 Configuration Report for more than 32 channels

The ASIPP table of the configuration report defines rows for up to 32 channels. We do not recommend to add more lines to this table if your system has more than 32 channels because this can lead to problems with VeriAnalyzer Program (resource limitation of Microsoft Word). Instead please use several configuration reports each listing up to 32 channels.
Example: verification of AMSY-6 chassis MB19 with 38 channels: fill out configuration report group 1 and 2 and name report like Veri01-32.cfg.doc. Copy this report and name it like Veri33-38.cfg.doc. Enter in Veri01-32.cfg.doc data of channel 1-32 and in Veri33-38.cfg.doc data of channel 33-38. In the VeriAnalyzer program you have to choose once Veri01-32.cfg.doc and once Veri33-38.cfg.doc for generating the ASIPP verification report ("ASIPP Start"-button). Consequently two ASIPP verification reports will be generated.

The split of the configuration report has only influence on the data analysis step with VeriAnalyzer.
Data acquisition for system verification (VeriStimulator) can be done in one step for all your channels.

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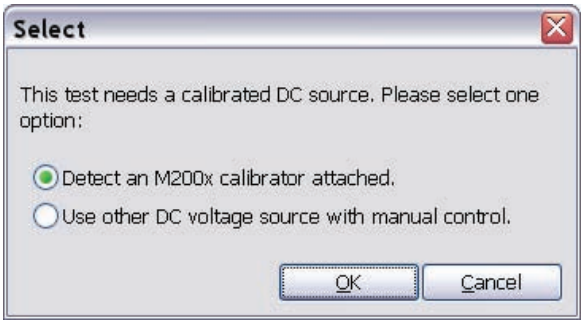
10.5 System Verification

The System Verification checks the PAx channels, the I/O flags and the Pulser.

10.5.1 Step 1: PAx, Flags

If a M200x DC calibrator is connected via serial interface select option 1 and continue.

If you have a manually controlled DC calibrator select option 2 and continue.


Select
This test needs a calibrated DC source. Please select one option:
Detect an M200x calibrator attached.
Use other DC voltage source with manual control.
OK
Cancel

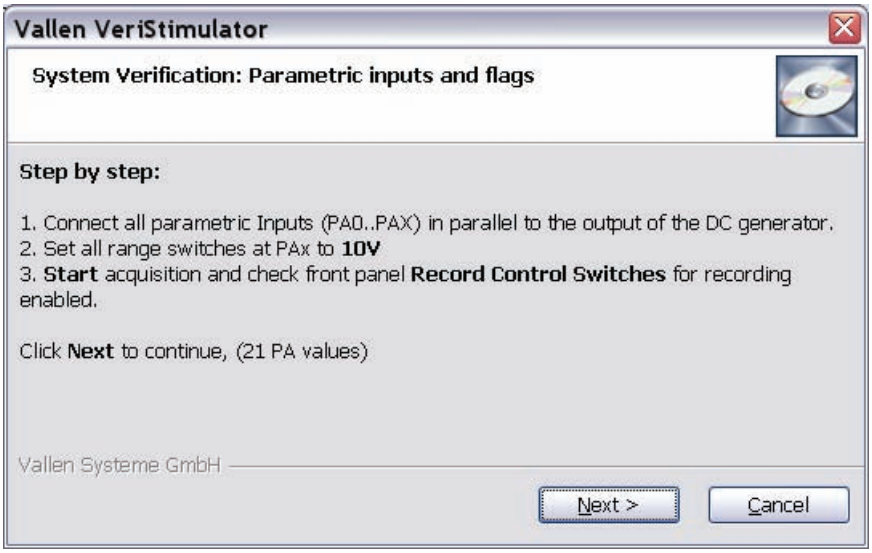
Connect all PAx channels in parallel to the DC calibrator.

Make sure that the PAx ranges are set to 10V.

Run the Acquisition program. Select a new vac-file and store it in the same folder you created during the "Create Veri-files…" step (we recommend file name of type *filename*.sys.vac).

Confirm the creation of a new file. For the settings browse to the folder containing the vac-file created during the step "Create Veri-Files…" and select it.

Make sure that the record control switches are in "enable" position.


Vallen VeriStimulator
System Verification: Parametric inputs and flags
Step by step:
1. Connect all parametric Inputs (PA0..PAX) in parallel to the output of the DC generator.
2. Set all range switches at PAx to 10V
3. Start acquisition and check front panel Record Control Switches for recording enabled.
Click Next to continue, (21 PA values)
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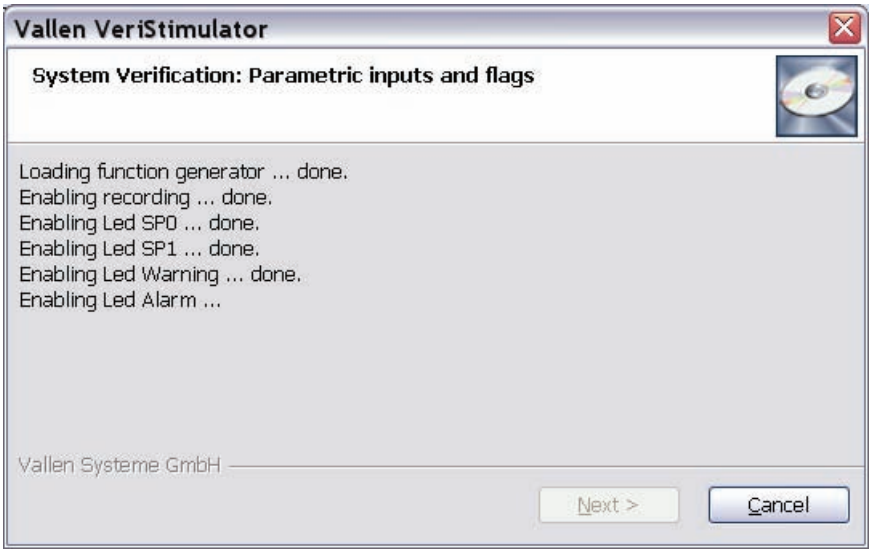
Next >
Cancel

In a next step the IO flags will be checked automatically.



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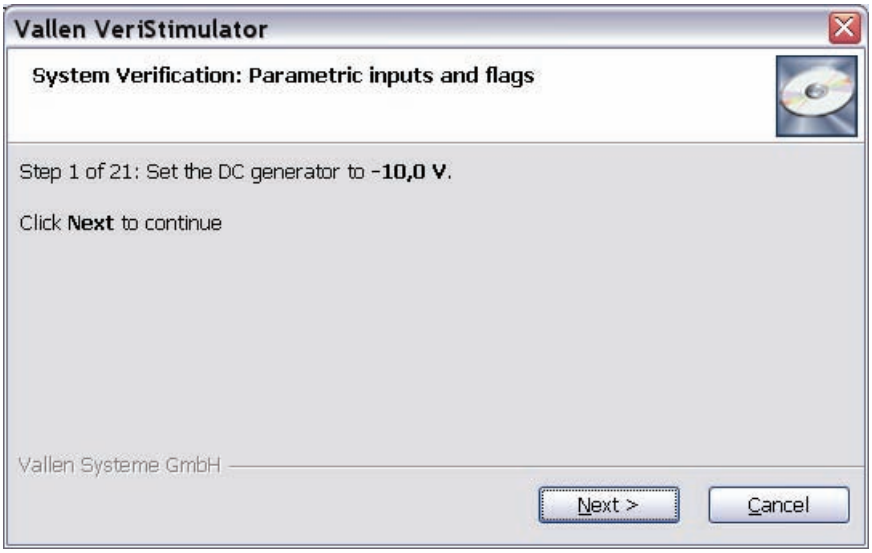
The first voltage that has to applied is -10V!

In case of the M200x one has to reverse polarity in order to get -10V. The PAx verification will run automatically until 0V is reached. Then you are prompted to provide positive voltage. To do so reverse polarity again.

If you are using a manually controlled DC calibrator, change the DC settings according to the instructions given in the pop up window.


Vallen VeriStimulator
System Verification: Parametric inputs and flags
Step 1 of 21: Set the DC generator to -10,0 V.
Click Next to continue
Vallen Systeme GmbH
Next >
Cancel

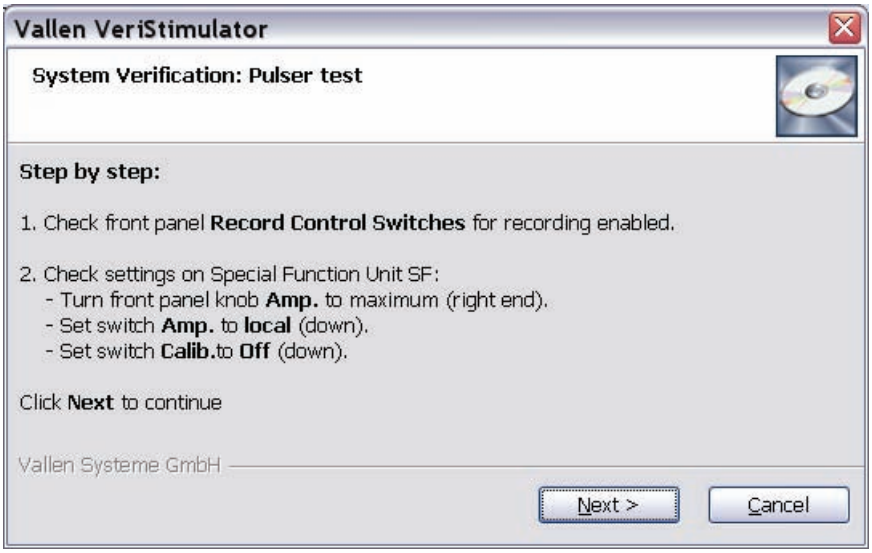
10.5.2 Step 2: Pulser

For this test you need the aforementioned (section 10.1) reference board. For the instructions about the reference board see section 10.1. Please select the correct filter settings for an ASIP-2 Reference Board (25-850kHz) or the dummy filters for an ASIPP board

Follow the instructions of the pop up window and make sure that the SF board switches and knobs are set correctly.

The “Amp.” knob has to be turned all the way to the right.

The “Amp.”-switch has to be set to local and the “Calib.” Switch has to be set to off.


Vallen VeriStimulator
System Verification: Pulser test
Step by step:
1. Check front panel Record Control Switches for recording enabled.
2. Check settings on Special Function Unit SF:
- Turn front panel knob Amp. to maximum (right end).
- Set switch Amp. to local (down).
- Set switch Calib.to Off (down).
Click Next to continue
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Next >
Cancel

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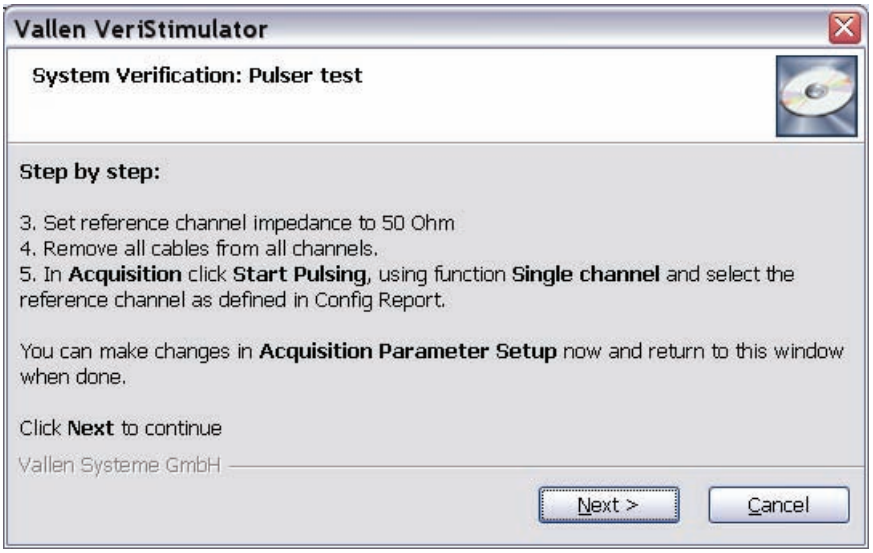
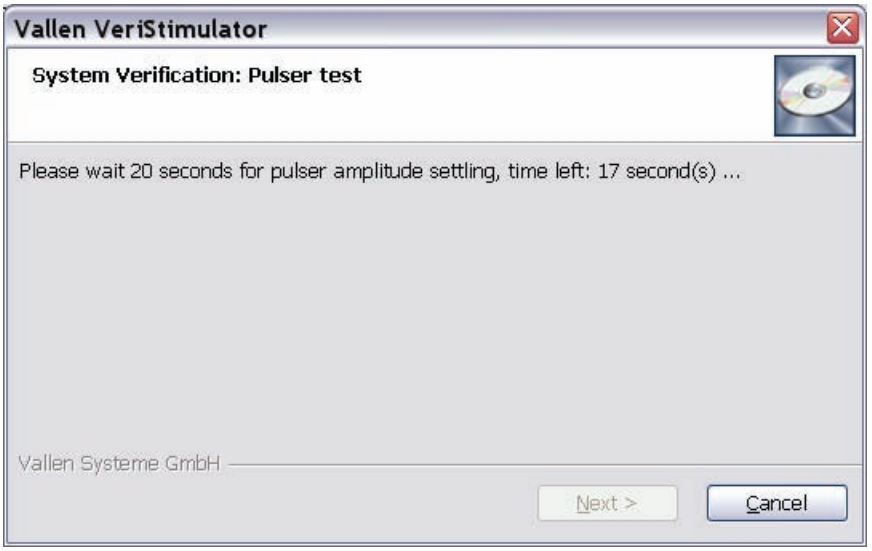
In the “Hardware Detection Results & Channel Configuration” dialog select an input device for the reference channel such as the ”AEP3-34dB-prog” or the “AEP4-34dB” or the “VS-150RIC (34dB)”. All these devices have an impedance of 50 Ohm and a gain of 34dB.

In acquisition start “Single Channel” pulsing and select the reference channel to send pulses.

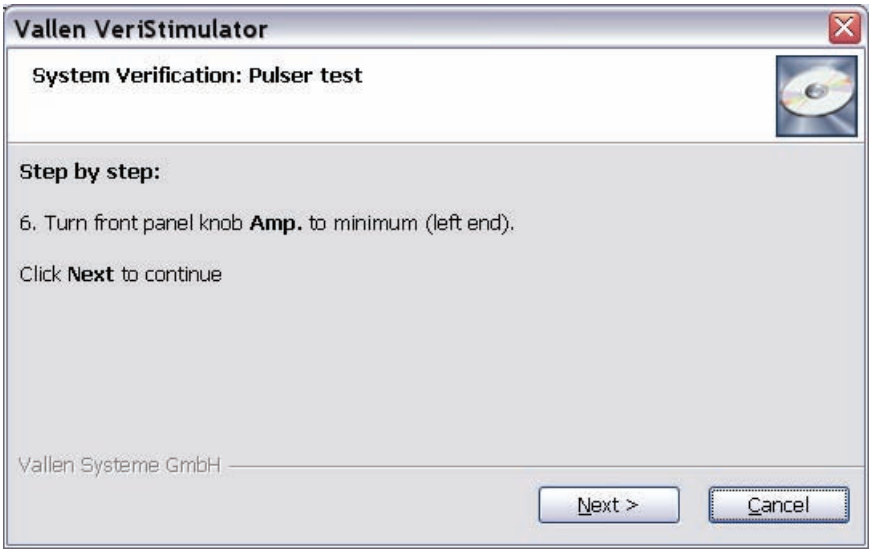

Vallen VeriStimulator
System Verification: Pulser test
Step by step:
3. Set reference channel impedance to 50 Ohm
4. Remove all cables from all channels.
5. In Acquisition click Start Pulsing, using function Single channel and select the reference channel as defined in Config Report.
You can make changes in Acquisition Parameter Setup now and return to this window when done.
Click Next to continue
Vallen Systeme GmbH
Next >
Cancel

Every time the pulser amplitude settings are changed, there is a delay of 20 seconds before the measurement is done. This lets the amplitude of the pulse settle.


Vallen VeriStimulator
System Verification: Pulser test
Please wait 20 seconds for pulser amplitude settling, time left: 17 second(s) ...
Vallen Systeme GmbH
Next >
Cancel

Next the minimum Amplitude of the pulser is verified.

Turn the front panel knob “Amp.” all the way to the left and continue.



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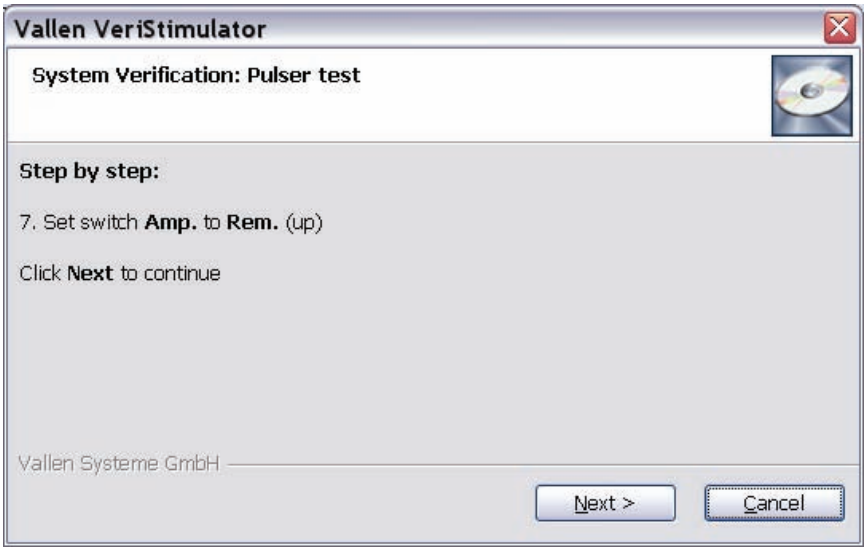
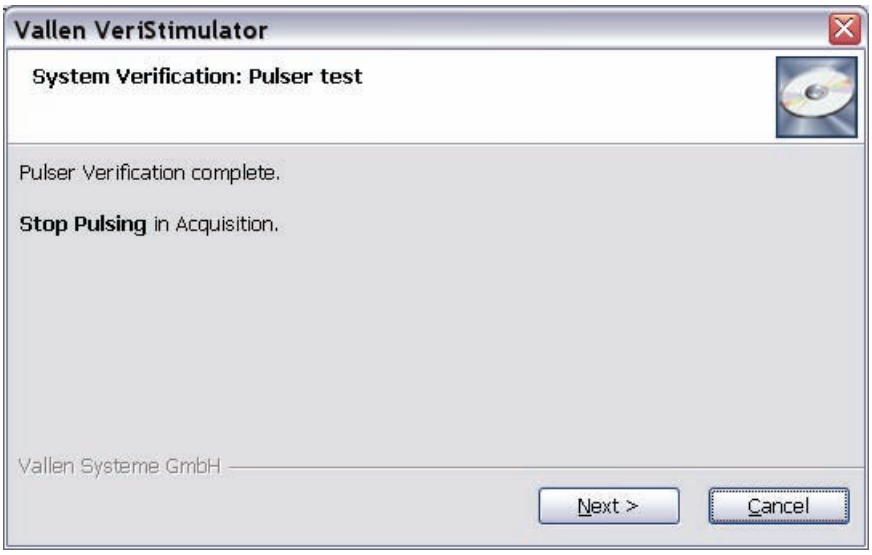
In the last step of the pulser verification the amplitude settings are controlled by software.

Set the “Amp.” switch to remote (“Rem.”) and continue.



Stop the pulsing in the Acquisition program after completion of the pulser verification



10.6 Channel Verification

If you installed a reference board for the Pulser test, remove it now. If the reference board was installed in place of an ordinary board you can put the original board back in again.

If your serial interface is occupied by the DC calibrator and you need such an interface to control the function generator you can unplug the DC calibrator. It is not needed for the channel verification procedure.
Before you start the channel verification, create a new vac-file. To do so stop the acquisition and select a new vac-file and store it in the same folder you previously created (we recommend file name of type *filename*.asip.vac). Confirm the creation of a new file.
For the AE-channel settings browse to the folder containing the vac-file created during the step “Create Veri-Files…” and select it.
Please also make sure that you selected an input device such as the ”AEP3-34dB-prog” or the “AEP4-34dB” or the “VS-150RIC (34dB)”. All these devices have an impedance of 50 Ohm and a gain of 34dB.
Make sure that in the VeriStimulator→Automatic Test tab→Parameters group, the

- “Working frequency” is set to a value well in between the high- and low pass filter (200kHz)
- RMS delay is set to 0 and
- Counter delay is set to 0

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During the channel verification you can set the “Audio” switch to the channel that is verified. During the data acquisition the noise will vary. You can adjust the volume and sensitivity with the according knobs at the SF-module (only AMSY-5).

10.6.1 Step 1: Test@Freq

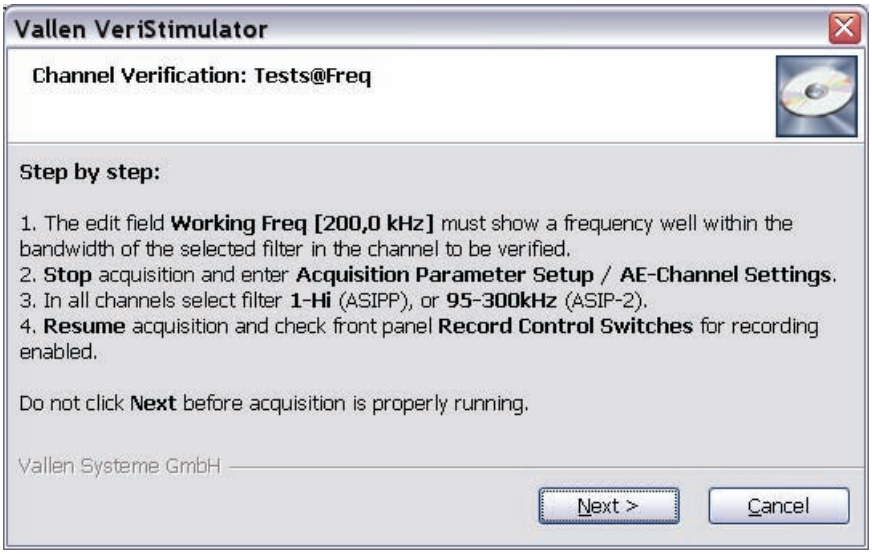
The working frequency has to be set well in between the interval specified by the filter settings in the AE-channel, e.g. to 200kHz for a 95-300kHz band pass filter.

ASIP-2 only:

Select filter 95-300kHz

ASIPP only:

Select filter 1-Hi.

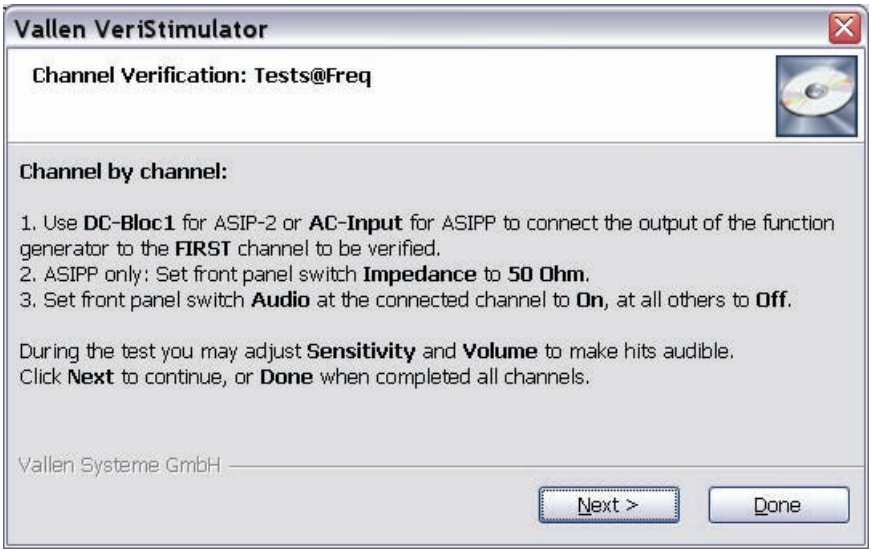

Vallen VeriStimulator
Channel Verification: Tests@Freq
Step by step:
1. The edit field Working Freq [200,0 kHz] must show a frequency well within the bandwidth of the selected filter in the channel to be verified.
2. Stop acquisition and enter Acquisition Parameter Setup / AE-Channel Settings.
3. In all channels select filter 1-Hi (ASIPP), or 95-300kHz (ASIP-2).
4. Resume acquisition and check front panel Record Control Switches for recording enabled.
Do not click Next before acquisition is properly running.
Vallen Systeme GmbH
Next >
Cancel

ASIP-2 only:

It is **VERY IMPORTANT** to use the DC-Bloc1. Otherwise the function generator will be damaged!

ASIPP only:

Use the AC-Input and make sure that “Impedance” switch is set to 50Ohm.


Vallen VeriStimulator
Channel Verification: Tests@Freq
Channel by channel:
1. Use DC-Bloc1 for ASIP-2 or AC-Input for ASIPP to connect the output of the function generator to the FIRST channel to be verified.
2. ASIPP only: Set front panel switch Impedance to 50 Ohm.
3. Set front panel switch Audio at the connected channel to On, at all others to Off.
During the test you may adjust Sensitivity and Volume to make hits audible.
Click Next to continue, or Done when completed all channels.
Vallen Systeme GmbH
Next >
Done

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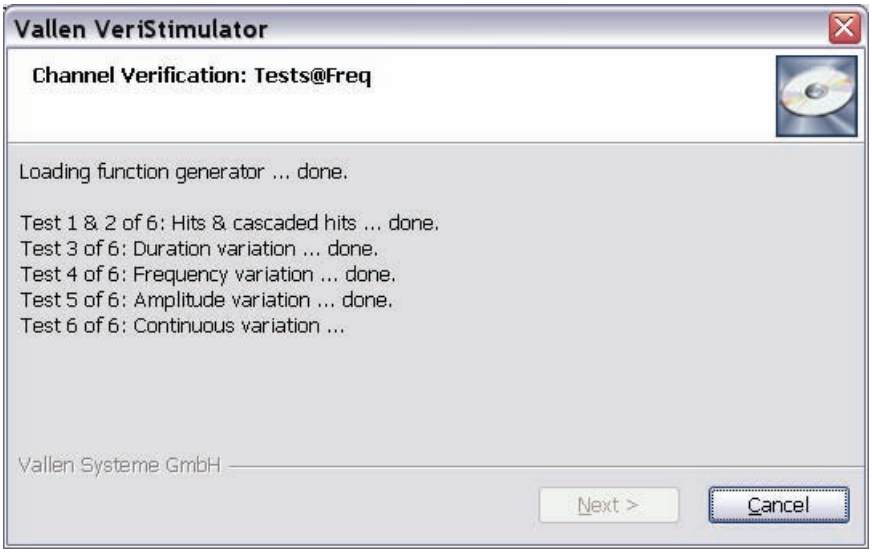
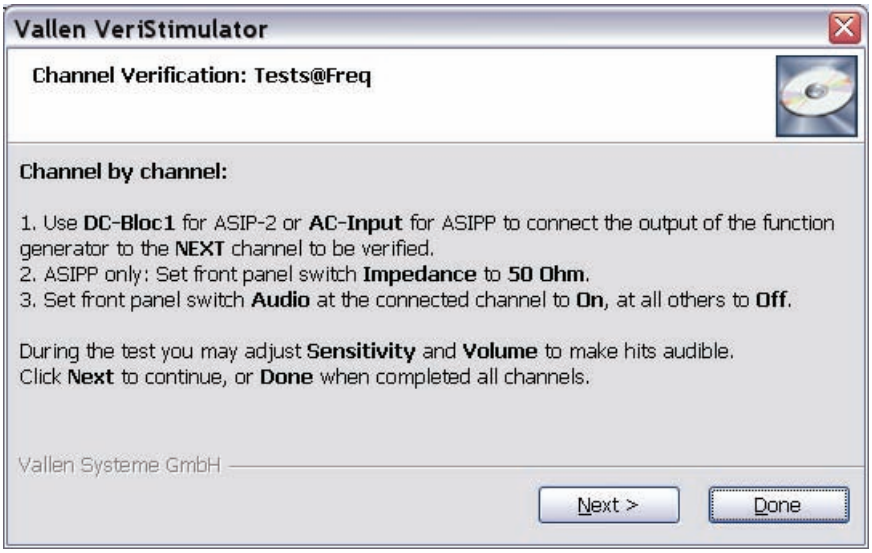
The test sequence runs automatically.


Vallen VeriStimulator
Channel Verification: Tests@Freq
Loading function generator ... done.
Test 1 & 2 of 6: Hits & cascaded hits ... done.
Test 3 of 6: Duration variation ... done.
Test 4 of 6: Frequency variation ... done.
Test 5 of 6: Amplitude variation ... done.
Test 6 of 6: Continuous variation ...
Vallen Systeme GmbH
Next >
Cancel

After completion of each channel you are prompted to connect the function generator to the next AE-channel.

Click “Done” to finish this verification step.


Vallen VeriStimulator
Channel Verification: Tests@Freq
Channel by channel:
1. Use DC-Bloc1 for ASIP-2 or AC-Input for ASIPP to connect the output of the function generator to the NEXT channel to be verified.
2. ASIPP only: Set front panel switch Impedance to 50 Ohm.
3. Set front panel switch Audio at the connected channel to On, at all others to Off.
During the test you may adjust Sensitivity and Volume to make hits audible.
Click Next to continue, or Done when completed all channels.
Vallen Systeme GmbH
Next >
Done

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10.6.2 Step 2: 2nd Filter

In order to test the 2nd filter, stop the Acquisition and enter the AE-Channel Settings.

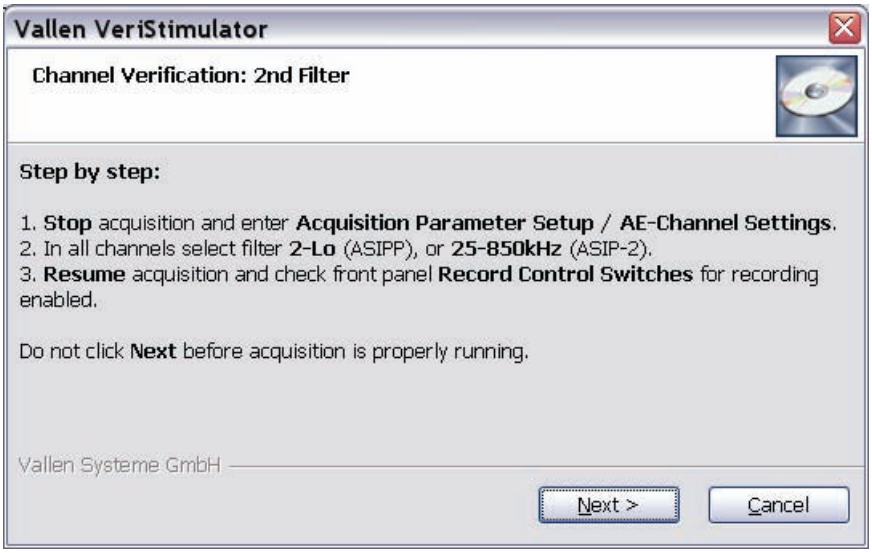
ASIP-2 only:

Select filter 25-850kHz

ASIPP only:

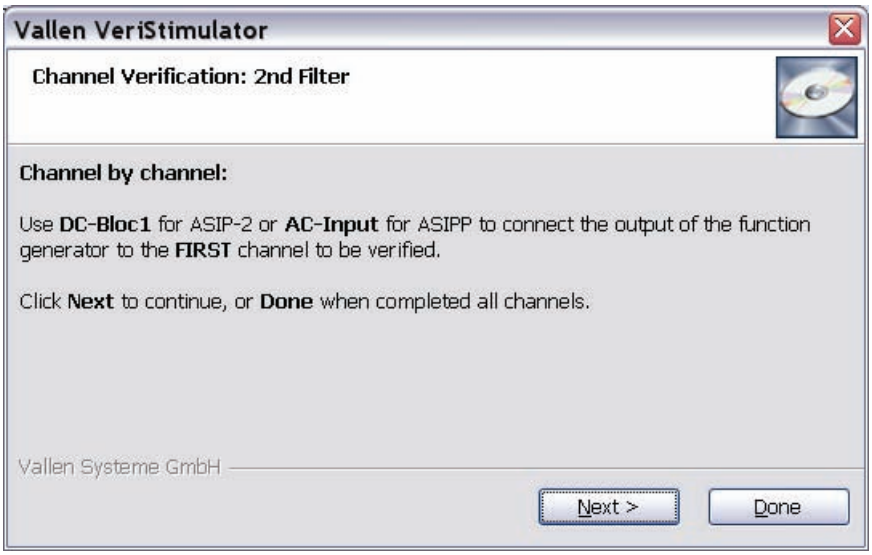
Select filter "2-Lo".

Start acquisition again and make sure that Record Control switches are on enable.

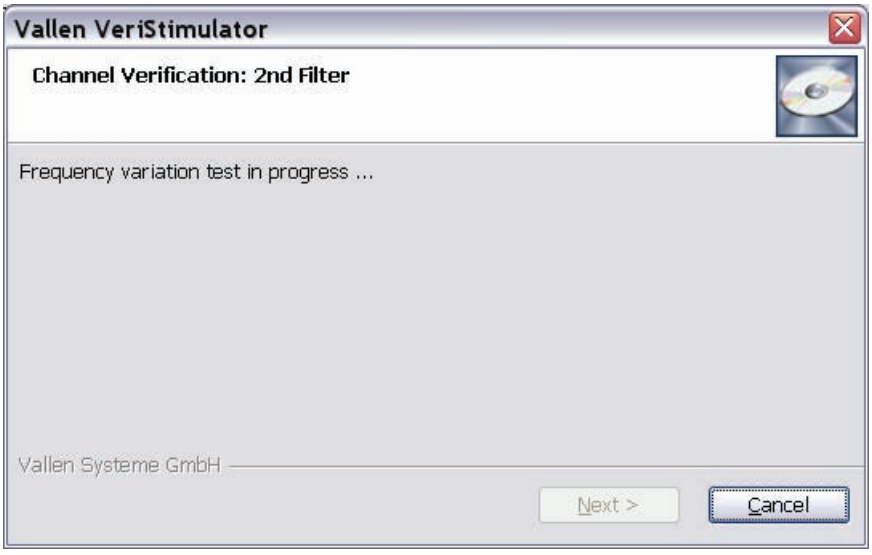

Vallen VeriStimulator
Channel Verification: 2nd Filter
Step by step:
1. Stop acquisition and enter Acquisition Parameter Setup / AE-Channel Settings.
2. In all channels select filter 2-Lo (ASIPP), or 25-850kHz (ASIP-2).
3. Resume acquisition and check front panel Record Control Switches for recording enabled.
Do not click Next before acquisition is properly running.
Vallen Systeme GmbH
Next >
Cancel

It is **VERY IMPORTANT** to use the DC-Bloc1. Otherwise the function generator will be damaged!

Use the AC-Input in case of an ASIPP board. For ASIPP boards make sure that "Impedance" switch is set to 50Ohm.


Vallen VeriStimulator
Channel Verification: 2nd Filter
Channel by channel:
Use DC-Bloc1 for ASIP-2 or AC-Input for ASIPP to connect the output of the function generator to the FIRST channel to be verified.
Click Next to continue, or Done when completed all channels.
Vallen Systeme GmbH
Next >
Done

No user action is required during this test.



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10.6.3 Step 3: Pulse through verification

This step checks whether the calibration pass works as expected.

Stop the acquisition and change the AE-channel filter settings.

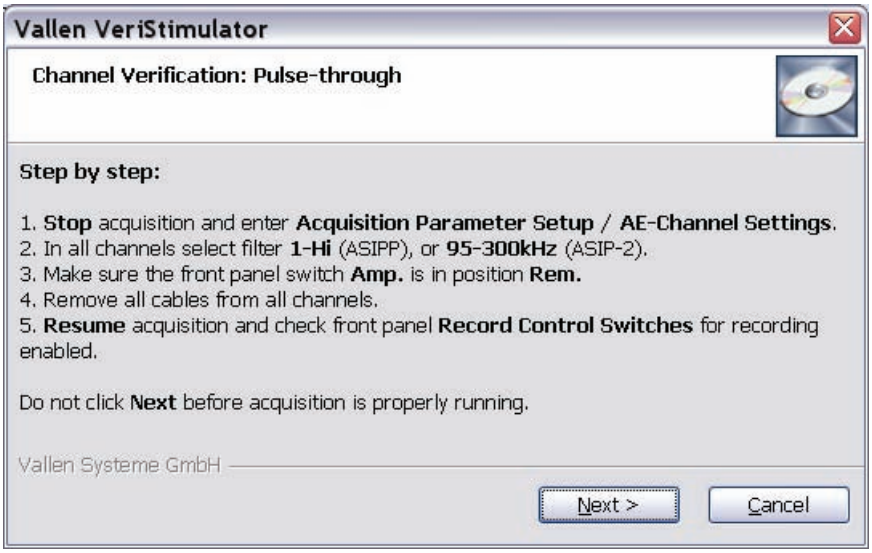
ASIP-2 only:

Select filter 95-300kHz

ASIPP only:

Select filter 1-Hi

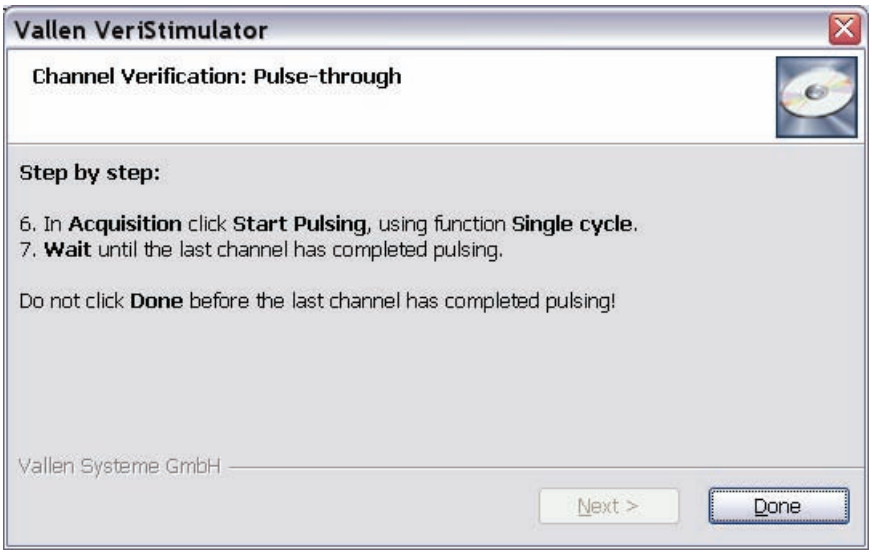
The front panel switch “Amp.” has to be in position “Rem.” (remote)


Vallen VeriStimulator
Channel Verification: Pulse-through
Step by step:
1. Stop acquisition and enter Acquisition Parameter Setup / AE-Channel Settings.
2. In all channels select filter 1-Hi (ASIPP), or 95-300kHz (ASIP-2).
3. Make sure the front panel switch Amp. is in position Rem.
4. Remove all cables from all channels.
5. Resume acquisition and check front panel Record Control Switches for recording enabled.
Do not click Next before acquisition is properly running.
Vallen Systeme GmbH
Next >
Cancel

Start the pulsing in acquisition: Single cycle.

The test ends after the last channel completed pulsing.

Click “Done” to finish this step of the SysVeri and to return to the VeriStimulator.


Vallen VeriStimulator
Channel Verification: Pulse-through
Step by step:
6. In Acquisition click Start Pulsing, using function Single cycle.
7. Wait until the last channel has completed pulsing.
Do not click Done before the last channel has completed pulsing!
Vallen Systeme GmbH
Next >
Done

10.7 Data Analysis for SysVeri

A printer can now be reconnected to LPT1 and the printer driver reconfigured to LPT1.

Start Vallen VeriAnalyzer (VeriAna.exe) from Vallen Control-Panel/Veri-Utilities. The menu in Fig. 21 appears.

In frame “Configuration file” browse to the Veri-Folder and select ‘filename.cfg.doc’.

In frame “Primary Data File for System Verification” browse to ‘filename.sys.pri’.
In frame “Primary Data File for ASIPP Verification” browse to ‘filename.asp.pri’.

Click on “System Start” to create the System Report. When processed, store the file on ‘filename.sys.doc’ and print it. Check and sign it.

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Click on “ASIPP Start” to create one page ASIPP-Report per channel. When processed, store the file on filename.ASP.doc and print it. Check and sign it.

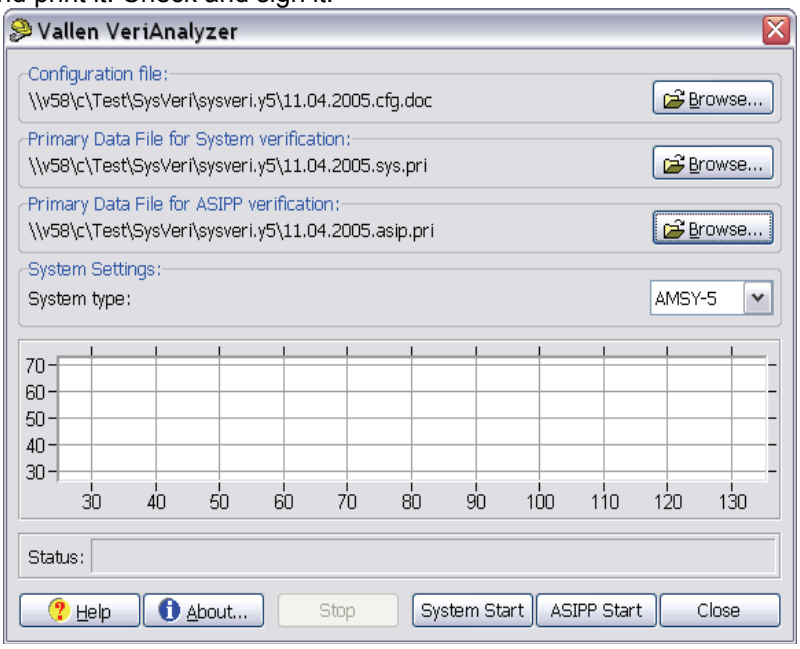

Fig. 21: VeriAnalyzer Menu

11 Verification Statistics and Pattern Lists

Vallen VeriAnalyzer gathers the results of all verifications in two files that reside in c:\vallen\SysVeri\.
File Sys.inc.txt contains results of system verifications,
File ASIPP.inc.txt contains results of ASIPP verifications.

These are text files that can easily be imported into an EXCEL sheet and used for e.g. statistical purposes.

During the data analysis, VeriAnalyzer creates two pattern list files in txt format in the Veri-Folder:

VeriSys.sys.txt contains the list of patterns checked during system verification, and
VeriASIPP.asp.txt contains the list of patterns checked during ASIPP verification.

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12 Verification of Transient Recorder

For the transient recorder verification the Vallen AMSY-5/AMSY-6 software package includes the TR-Tester software that can be started from Vallen-Control-Panel, Tab Veri-Utilities.

This program is almost identical to Vallen Acquisition program, uses the same routines with the following essential changes:

- Instead of ADC data, a sequence of predefined patterns is stored in the transient recorder hardware with each trigger of a channel (trigger by threshold crossing as usual)
- Instead of storing the data on file, the hardware generated patterns are compared by the software and in case of any deviation, an error is reported.
- Acquisition settings are program defined and change with test progress. All sampling rates and all record lengths are tested in a predefined sequence.
-
- The program setup is self explaining and easy to use.

13 Vallen VeriStimulator in Manual Mode.

The VeriStimulator and arbitrary function generator can also be used in a manual mode. The operator can vary amplitude, frequency, and the envelope function of a burst. It is also possible to create short pulses down to 50ns width and pulse trains (e.g. N pulses in distance of t µs) to verify system response in such situations.

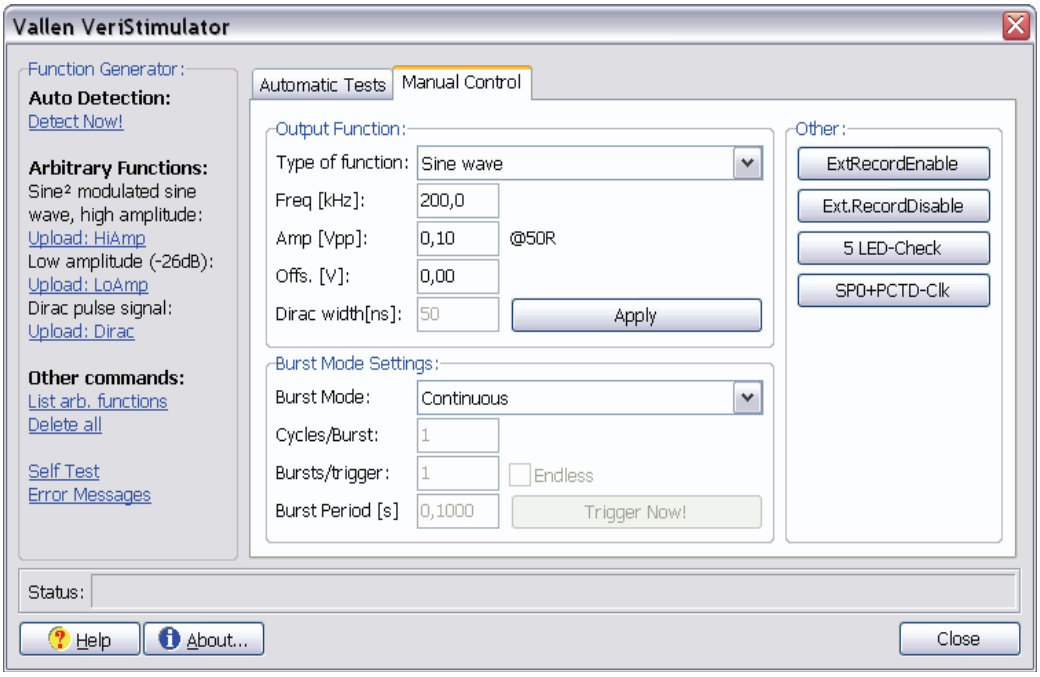

Fig. 22: VeriStimulator in Tab Manual Control

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13.1 Type of function

The selection box next to “Type of function” offers eight alternatives:
Sine wave, Square wave, Triangle wave , Ramp wave, Noise, Dirac, Sin^2-HiAmp, Sin^2-LoAmp.

The first 5 alternatives are hard coded in the function generator. The last three refer to the special waveforms loaded into the non-volatile memory of the function generator by VeriStimulator.

With the function “**Dirac**” a sharp and short pulse of 50ns or greater can be produced.
With function “**Sin^2-HiAmp**” the sine-square modulated sine wave of Fig. 9 can be produced. The amplitude range is 50mV to 10Vpp at 50R. Sin^2-LoAmp generates the same function but 26dB less in amplitude than what is entered in the amplitude field.

13.2 Burst Mode Settings

The selection box next to “Burst Mode” offers three alternatives:
Continuous, Burst (FG), Burst (SW).

Select continuous mode for a continuous sine wave, square wave, triangle wave, ramp wave, or for continuous noise.
Burst example: A rectangle gated burst of 1ms duration and 200kHz frequency:
Select “Sine wave” and “Burst (FG)”. In field “cycles/burst” enter the duration of the burst in number of full waves (cycles). At a frequency of 200kHz, a cycle lasts 5µs. For a burst of 1 ms, define 200 cycles per burst.

When the check box “Endless” is NOT checked, the function generator produces one burst per click on “Trigger Now”. For a periodic repetition of bursts, enter the desired burst period and check “endless” and click once “Trigger Now”.

For a periodic trigger of the Sine-square modulated sine wave of Fig. 9, or the Dirac pulse, select the mode “Burst (SW)”. SW means that the periodic trigger is generated by software. Click on “Trigger Now” to trigger one burst. Check “Endless” to produce periodic bursts in the defined burst period. Burst (SW) supports a minimum burst period of about 1 second.

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14 Appendix: Verification of AMSY-6

This appendix is an addition to the previous chapters and describes points which must be observed when using the SysVeri Software R2011.0303 or later for AMSY-6. The verification of the AMSY-6 is not yet fully integrated in the SysVeri software and the previous chapters. Nevertheless it is possible to verify AMSY-6 with SysVeri by taking the points described in this chapter into account. Only the differences to AMSY-5 verification are described in this chapter. For description of overall proceeding of system verification please see previous chapters.

14.1 Overview

With respect to using SysVeri software the main differences between AMSY-5 and AMSY-6 are:

- In the configuration report (see chapter 10.4) please enter as system box type the chassis type of your AMSY-6 (MB2, MB6, or MB19).
- Input range of parametric channels is set in AMSY-5 by HW-switch “1V/10V” and in AMSY-6 by software. Since the verification must be done with input range 10V, the input range must be set by software before starting “System Verification, Step 1: PAx, Flags”.
- The amplitude of the pulser can be set in AMSY-5 by HW-knob or by software (switch “Rem./Local” set to “Rem.”) whereas in AMSY-6 the pulser parameters are set only in software by “DAC online control” during acquisition. This has an impact on “System Verification, Step2: Pulser” because the amplitude of the pulser must be set by software during acquisition.

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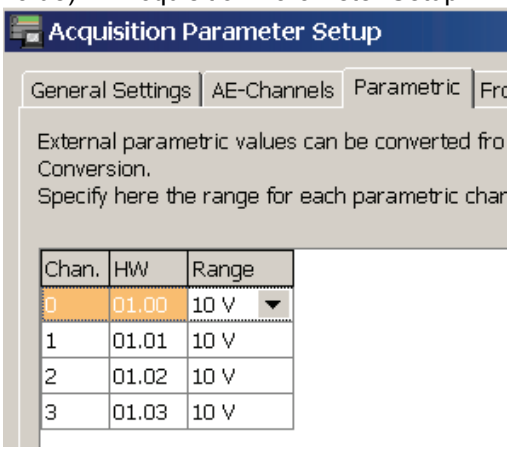
14.2 System Verification, Step1: PAx, Flags

Corresponding chapter for AMSY-5 is chapter 10.5.1.
The following table shows where special actions are necessary for the AMSY-6 Acquisition

Steps in VeriStimulator / Info given by VeriStimulator	**Vallen Acquisition program with AMSY-6 connected:**
Start System Verification/Step1: PAx, Flags **Step by step:** 1. Connect all parametric Inputs (PA0..PAX) in parallel to the output of the DC generator, for negative input. 2. Set all range switches at PAx to **10V** 3. **Start** acquisition and check front panel **Record Control Switches** for recording enabled. Click **Next** to continue, (21 PA values).	Concerning item "2. Set all range switches at PAx to 10V" (see on the left): on AMSY-6 no HW-switches for the parametric channels exist. Instead the input range of the parametric channels must be set by software to 10V. Before starting data acquisition with "Go to data acquisition" set the input range of the parametric channels to 10 V (usually default value) in "Acquisition Parameter Setup":  Then "Go to data acquisition" and continue as instructed by the VeriStimulator window.

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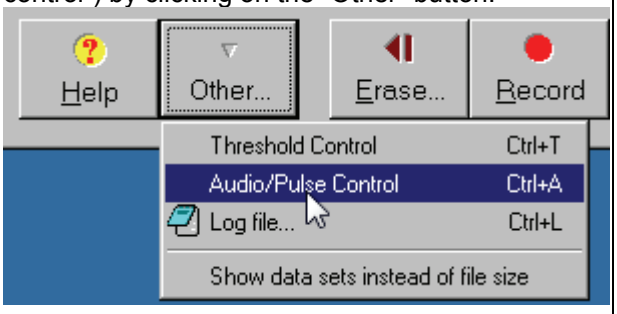
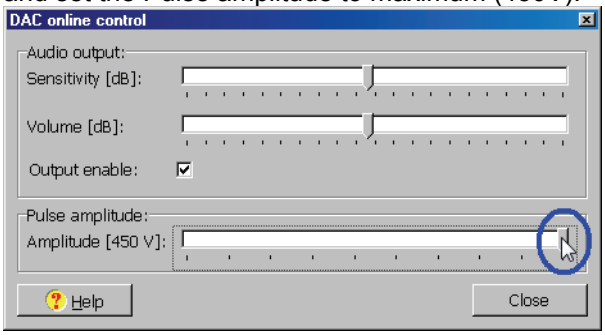
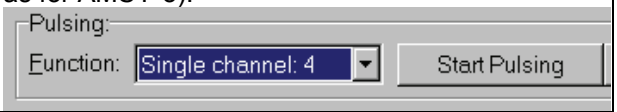
14.3 System Verification, Step2: Pulser

Corresponding chapter for AMSY-5 is chapter 10.5.2.

Steps in VeriStimulator / Info given by VeriStimulator	**Vallen Acquisition program with AMSY-6 connected:**
Start System Verification/Step2: Pulser **Step by step:** 1. Check front panel **Record Control Switches** for recording enabled. 2. Check settings on Special Function Unit SF: - Turn front panel knob **Amp.** to maximum (right end). - Set switch **Amp.** to **local** (down). - Set switch **Calib.**to **Off** (down). Click **Next** to continue.	Set the frequency filter settings of your reference ASIP-2 board to 25-850 kHz (Acquisition Parameter Setup). Concerning item 2 “Check settings on Special Function Unit SF” (see on the left) must be ignored: on AMSY-6 no HW-knob is present to set manually the amplitude of the pulser; the switch “AMP.” does not exist because the pulser is always controlled remotely by software; the switch “Calib.” does not exist – pulsing can be only started by software. Start acquisition with “Go to data acquisition”. Open the Audio/Pulse Control (“DAC online control”) by clicking on the “Other” button.  and set the Pulse amplitude to maximum (450V):  The Audio output parameters play no role for automatic verification.
Step by step: 3. Set reference channel impedance to 50 Ohm (ASIPP only). 4. Set reference channel filter to 25-850kHz. 5. Remove all cables from all channels. 6. In **Acquisition** click **Start Pulsing**, using function **Single channel** and select the reference channel as defined in Config Report. You can make changes in **Acquisition Parameter Setup** now and return to this window when done. Click **Next** to continue.	Item 4 has been done already before (see above), i.e. you can ignore it here. For Item 6 select single channel with reference channel (e.g. 4 in screenshot below) and click “Start Pulsing”. (same as for AMSY-5): 
Step by step: 7. Turn front panel knob **Amp.** to minimum (left end). Click **Next** to continue.	Instead of Item 7 set pulse amplitude in “DAC online control” to minimum before clicking “next” in the VeriStimulator.

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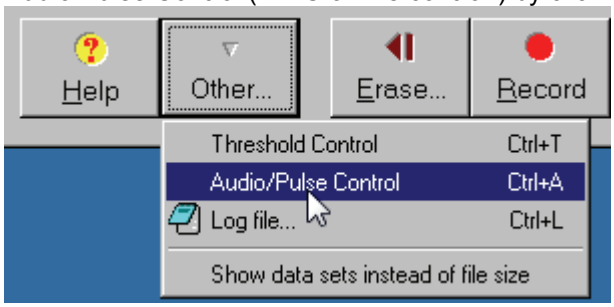
Steps in VeriStimulator / Info given by VeriStimulator	Vallen Acquisition program with AMSY-6 connected:
Step by step: 8. Set switch **Amp.** to **Rem.** (up) Click **Next** to continue.	Set pulse amplitude in “DAC online control” to 200V. You can use the “move left”/”move right” keys to position exactly after selecting the ruler with the mouse. Ignore Item 8 “Set switch AMP. to Rem. (up)” because this switch does not exist on AMSY-6:
Pulser Verification complete. **Stop Pulsing** in Acquisition.	No difference to AMSY-5.

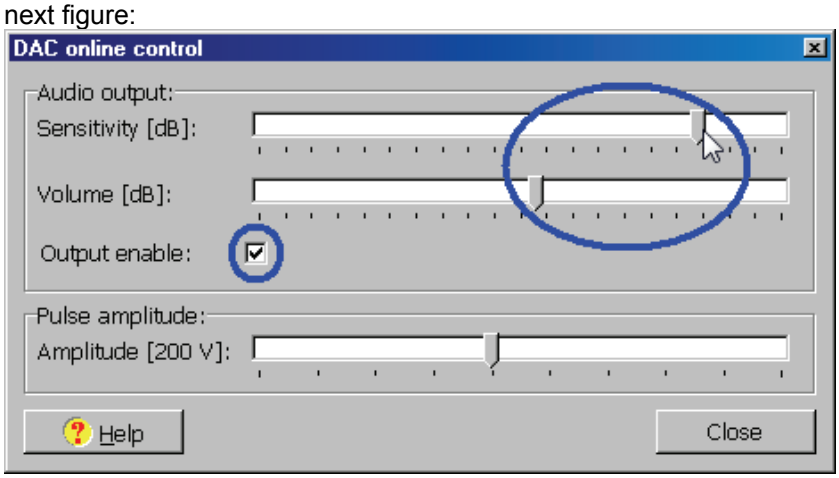
14.4 Channel Verification

14.4.1 Audio control

Corresponding chapter for AMSY-5 is chapter 10.6.
As described in chapter 10.6, you may set the “Audio” switch to the channel that is verified. During the data acquisition the noise will vary. In contrast to the description in chapter 10.6, no knobs exist on the AMSY-6 to adjust volume and sensitivity of the audio output. For this purpose please open instead during acquisition the Audio/Pulse Control (“DAC online control”) by clicking on the “Other” button:



Then enable “Output enable” and use the rulers for Audio output in the “DAC online control” as shown in next figure:



Please note that for high sensitivity you have to move the upper ruler to the right.
The chassis MB2 does not have a built-in loudspeaker. Instead you can connect passive stereo loudspeakers to the speaker connector at the rear.
Please do not change the pulse amplitude value of 200V because this value is needed for “Pulse through verification step”.

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14.4.2 Channel verification, Step 3: Pulse through verification

Corresponding chapter for AMSY-5 is chapter 10.6.3.
Chapter 10.6.3 describes that you have to set the front panel switch “Amp.” to position “Rem”. This instruction you can ignore, because on AMSY-6 this switch does not exist and the pulser amplitude is always controlled by software. The pulser amplitude is set by the SysVeri acquisition setup file to 200V which is the value needed for this verification step. You can control this value by the “DAC online control” (see previous section).

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